

Specifications

Parameter	Value																				
OFET																					
Substrate (Gate)	n-doped silicon (doping at wafer surface: $n \sim 3 \cdot 10^{17} \text{ cm}^{-3}$), 150 mm wafer according to SEMI standard ($675 \pm 20 \mu\text{m}$ thickness)																				
Gate Oxide	$230 \pm 10 \text{ nm SiO}_2$ (thermal oxidation) Other oxide thicknesses (90 ... 500 nm) can be realized upon request																				
Contacts (Drain/Source)	30 nm Au with 10 nm high work function adhesion layer (ITO) (structured by lift-off technique)																				
Test Chip Size	$15 \times 15 \text{ mm}^2$																				
Test Chip Transistor Configurations	<table border="0"> <tr> <td></td> <td>Gen. 4</td> <td>Gen. 5</td> <td>Customer Layout</td> </tr> <tr> <td>4 transistors L = 2.5 μm</td> <td>W = 10 mm</td> <td>W = 2 mm</td> <td rowspan="5">available upon request</td> </tr> <tr> <td>4 transistors L = 5 μm</td> <td>W = 10 mm</td> <td>W = 2 mm</td> </tr> <tr> <td>4 transistors L = 10 μm</td> <td>W = 10 mm</td> <td>W = 2 mm</td> </tr> <tr> <td>4 transistors L = 20 μm</td> <td>W = 10 mm</td> <td>W = 2 mm</td> </tr> <tr> <td>Contact pads $0.5 \times 0.5 \text{ mm}^2$</td> <td></td> <td></td> </tr> </table>		Gen. 4	Gen. 5	Customer Layout	4 transistors L = 2.5 μm	W = 10 mm	W = 2 mm	available upon request	4 transistors L = 5 μm	W = 10 mm	W = 2 mm	4 transistors L = 10 μm	W = 10 mm	W = 2 mm	4 transistors L = 20 μm	W = 10 mm	W = 2 mm	Contact pads $0.5 \times 0.5 \text{ mm}^2$		
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Contact pads $0.5 \times 0.5 \text{ mm}^2$																					
Shipment Type	Diced wafer (60 test chips at $15 \times 15 \text{ mm}^2$) on foil with air tight packaging Resist protection layer AZ7217 (soluble in AZ thinner or acetone)																				
OFET (trimmed)																					
Substrate (Gate)	n-doped silicon (doping at wafer surface: $n \sim 3 \cdot 10^{17} \text{ cm}^{-3}$), 150 mm wafer according to SEMI standard ($675 \pm 20 \mu\text{m}$ thickness)																				
Gate Oxide	$230 \pm 10 \text{ nm SiO}_2$ (thermal oxidation) Other thicknesses from 10 nm to 500 nm are available upon request																				
Test Chip Size	$15 \times 15 \text{ mm}^2$ (standard), other sizes are available upon request																				
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LOFET																					
Wafer	150 mm according to SEMI standard																				
Structure Classes	11 transistors, 4 inverters and 4 ring oscillators; additional technology test structures																				
Die Size	$15 \times 15 \text{ mm}^2$																				
Number of Dies	60																				
Number of Pads	39 + 2																				
Pad Size	$1200 \times 800 \mu\text{m}^2$																				
Gate Oxide	$200 \pm 10 \text{ nm}$																				
Structured Layers	3 (gate, contacts, drain/source)																				
Source/Drain Layer	Ti/TiN, R_s approx. $10 \Omega/\text{sq}$.																				
Contacts	Standard $20 \times 20 \mu\text{m}^2$, R approx. 20Ω																				
Top Layer	70 nm Au with 10 nm high work adhesion layer (ITO, structured by lift-off technique) R_s approx. $0.65 \Omega/\text{sq}$. / $0.45 \Omega/\text{sq}$.																				
Shadow Mask	possible, but not required																				
Probecard	possible, but not required																				
Shipment Type	Diced wafer (60 test chips) on foil with air tight packaging Resist protection layer AZ7217 (soluble in AZ thinner or acetone)																				
OFET Miniprober																					
Size	$120 \text{ mm} \times 110 \text{ mm} \times 35 \text{ mm}$																				
Wight	280 g																				
Material	Body: Aluminium, PCB: FR4																				
Contacts	Top side: spring contacts, gold plated, 0.33 mm diameter; Back side: FR4, gold plated																				
Connector	3 \times BNC, Triaxial upon request																				
Functionality	Up-down movement of a thread and adjusting knob Warning! Do not use with hazardous voltages (>100V)																				