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FRAUNHOFER INSTITUTE FOR PHOTONIC MICROSYSTEMS IPMS

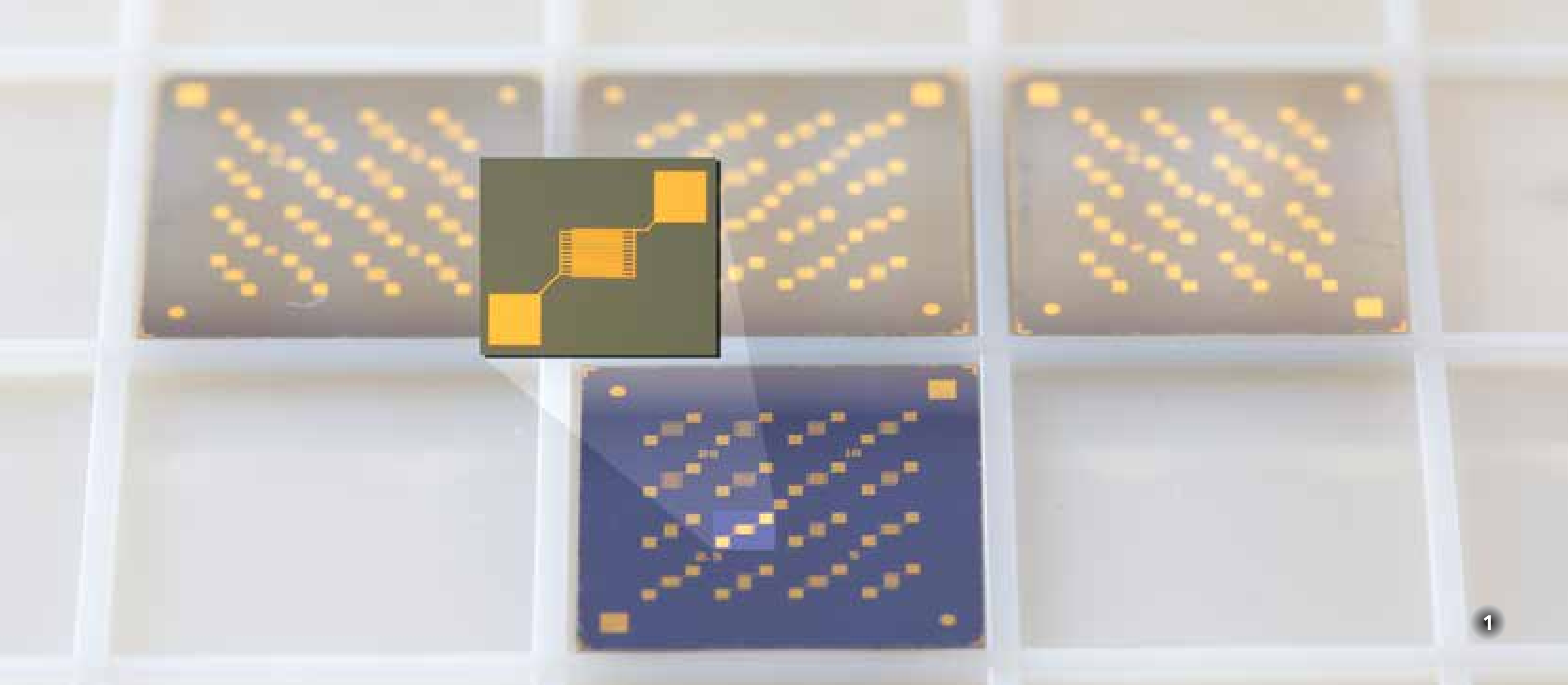
END-OF-LINE STANDARD SUBSTRATES FOR THE CHARACTERIZATION OF ORGANIC SEMICONDUCTOR MATERIALS

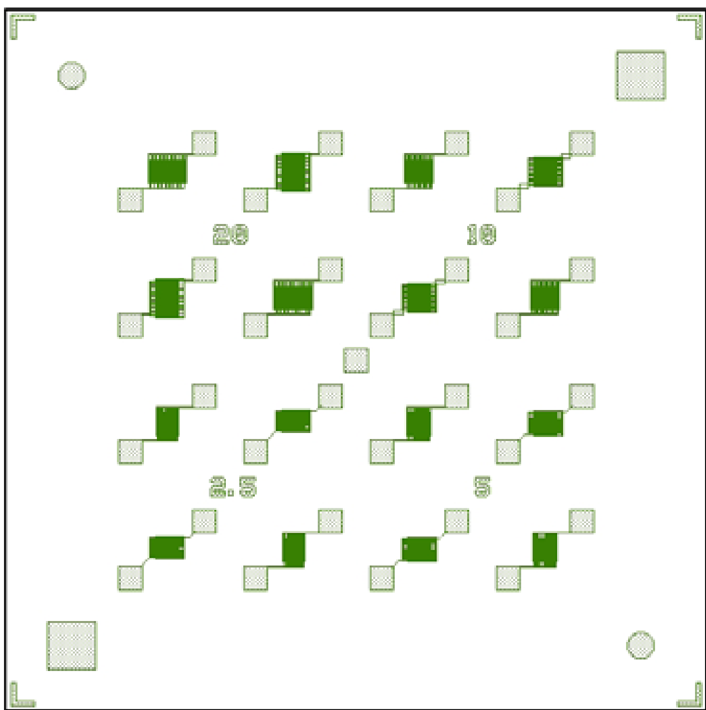
Over the last few years, organic electronics have become a keyword for new types of applications based on organic semiconductors and other materials that can easily be processed. Typical for this new class of materials are low temperature processes and large area deposition and structuring with various coating and printing processes. The active semiconductor materials determine the performance of the entire system considerably. That is why a simple and reliable electronic characterization of these semiconductors is not only an essential prerequisite for material development in the labs of organic chemists but also for process developers and circuit designers.

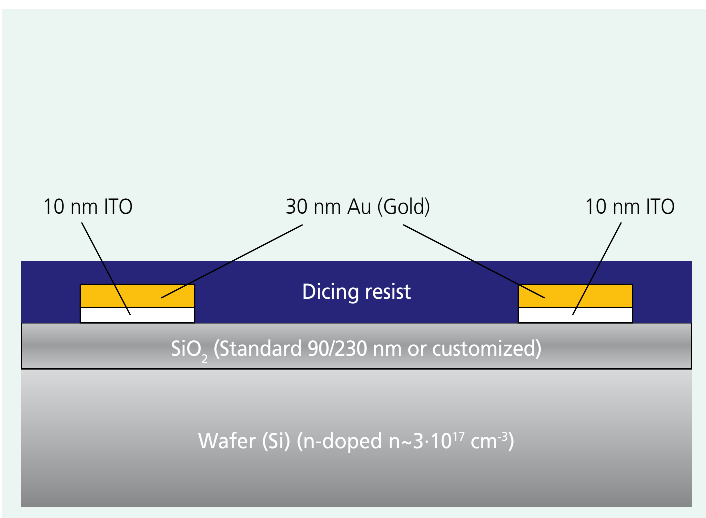
For material analysis in the field of organic semiconductors, the Fraunhofer IPMS provides standardized single transistor structures in bottom gate architecture. These substrates for organic field effect transistors (OFETs) are produced in the clean room on silicon wafers with thermal silicon dioxide (SiO_2) as full-area dielectrics and gold electrodes in lift-off technology. This is a significant advantage with respect to reliability and reproducibility that enables the application of these substrates for quality assurance in major chemical corporations.

The spectrum of possible customers is very large and ranges from universities, independent research institutions to industrial customers. The OFET substrates that are manufactured are used for research purposes in the field of materials testing or for quality control, respectively. They are essential for organic materials development. To date, the customer base of Fraunhofer IPMS in this sector has grown to 100 customers worldwide, including 15 key customers and two market-listed companies, both national and international.

The Fraunhofer IPMS offers different standard solutions and realizes customer-specific modifications by tailoring the samples with respect to chip size, design, and layer thickness of the thermal oxide. In order to simplify the measurement procedures of OFET substrates, the Fraunhofer IPMS has also developed a hand prober. This OFET miniprober allows faster and easier measurements by reliable pad contacting.





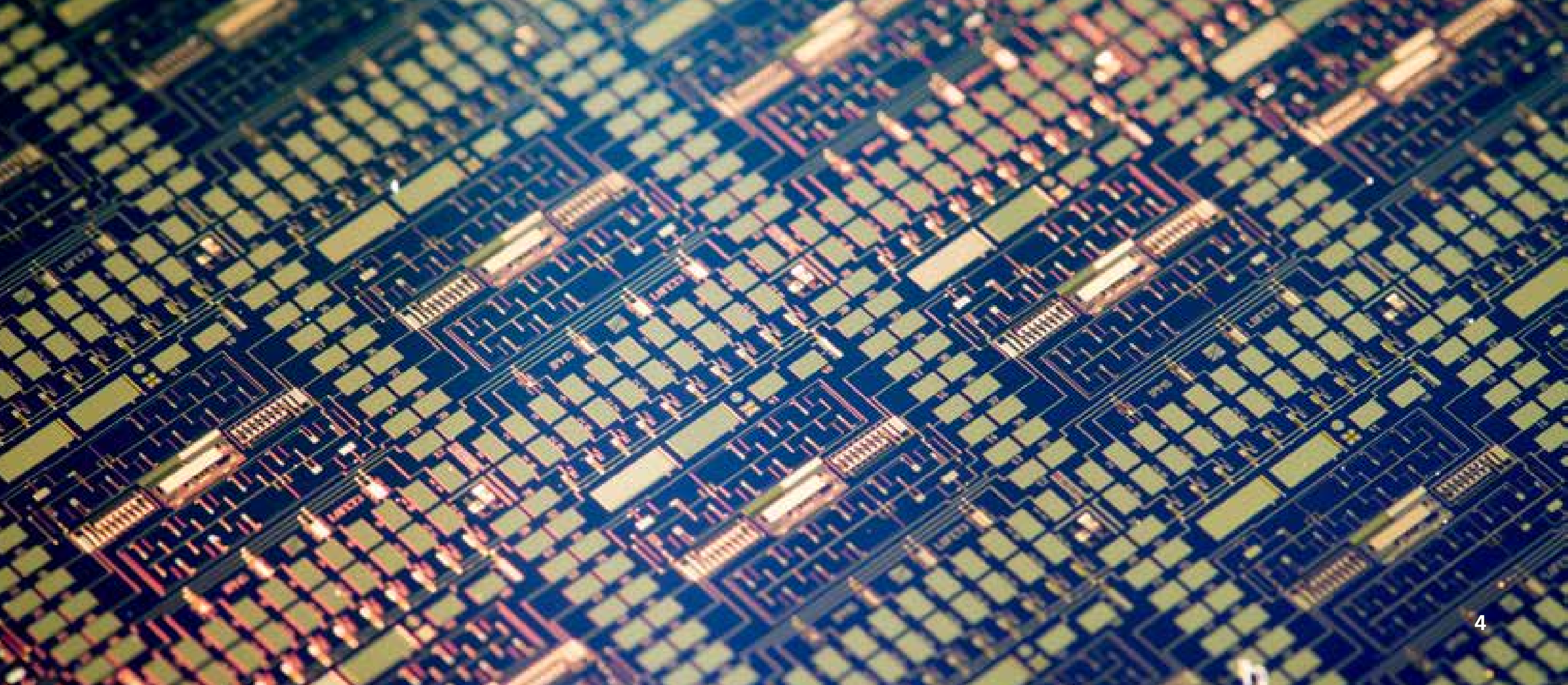


Organic Field Effect Transistors (OFET)

If an organic semiconductor layer is deposited on such a substrate, the Si-bulk acts as gate electrode and controls the channel current between the gold electrodes on top. A suitably doped Si-SiO_2 interface in CMOS quality guarantees a reproducible gate contact. Gold electrodes with a patented undercoating suppress the formation of injector barriers between the gold electrodes and the organics in the transistor channel. This guarantees reliable ohmic source/drain contacts in the OFET even for p-type semiconductors. Due to both reliability and reproducible preparation, these substrates are applied for standardized material screening by all key developers of organic semiconductors all over the world.

In the standard OFET layout, each 150 mm wafer has 960 individual transistors on 60 chips, each sized at 15 × 15 mm². Each chip carries four groups with four identical transistors, with a channel length of 2.5, 5, 10 and 20 µm respectively (Figure 2). Identical layouts with graded channel widths as well as a flexible selection of the oxide thickness allow the adjustment to a broad voltage and conductivity range of the test materials. Customer-specific layouts with different electrode geometries are possible at any time.

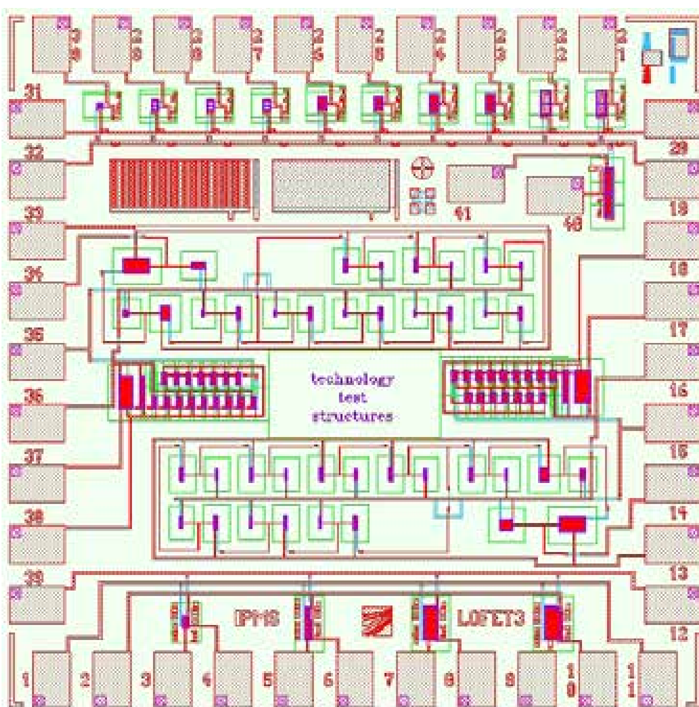
1 *OFET Chips (Inset: Single Transistor)*
2 *OFET Chip Layout*
3 *OFET Waferstack*

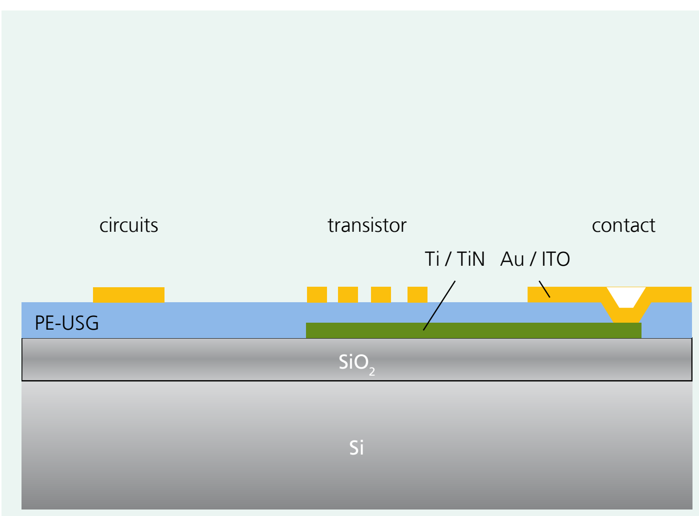


Basic Logic Circuits with Lateral Organic Field Effect Transistors (LOFET)

One further step in simplifying materials characterization is the analysis of basic logic circuits. Here, up to 36 single transistors are interconnected to inverters and ring oscillators. Monitoring of the active materials then only requires a frequency measurement of the ring oscillators which can be automated easily. This prevents the complicated and time-consuming measurement and analysis of the individual transistor characteristic. Furthermore, it is not only reliable information about logic capability that is acquired. The dynamic characteristics of the inverters are also determined.

The layout of a LOFET chip (Figure 5) includes an initial block with eleven individual transistors making a complete parameter extraction for circuit simulation possible. A second block contains four inverters which are replicated in the oscillators. These separately accessible inverter levels enable a detailed analysis of the transient behavior in case the amplification of the individual inverter stages is not sufficient for starting the oscillation of the ring oscillators. The third block contains ring oscillators with either seven or 15 stages. Each ring circuit has a three-stage output amplifier which decouples the oscillation inside the ring from the output terminal and allows a direct frequency measurement without external amplification. The LOFET substrates are also produced in bottom gate architecture so that functional circuits require the deposition of the semiconductor layer only.

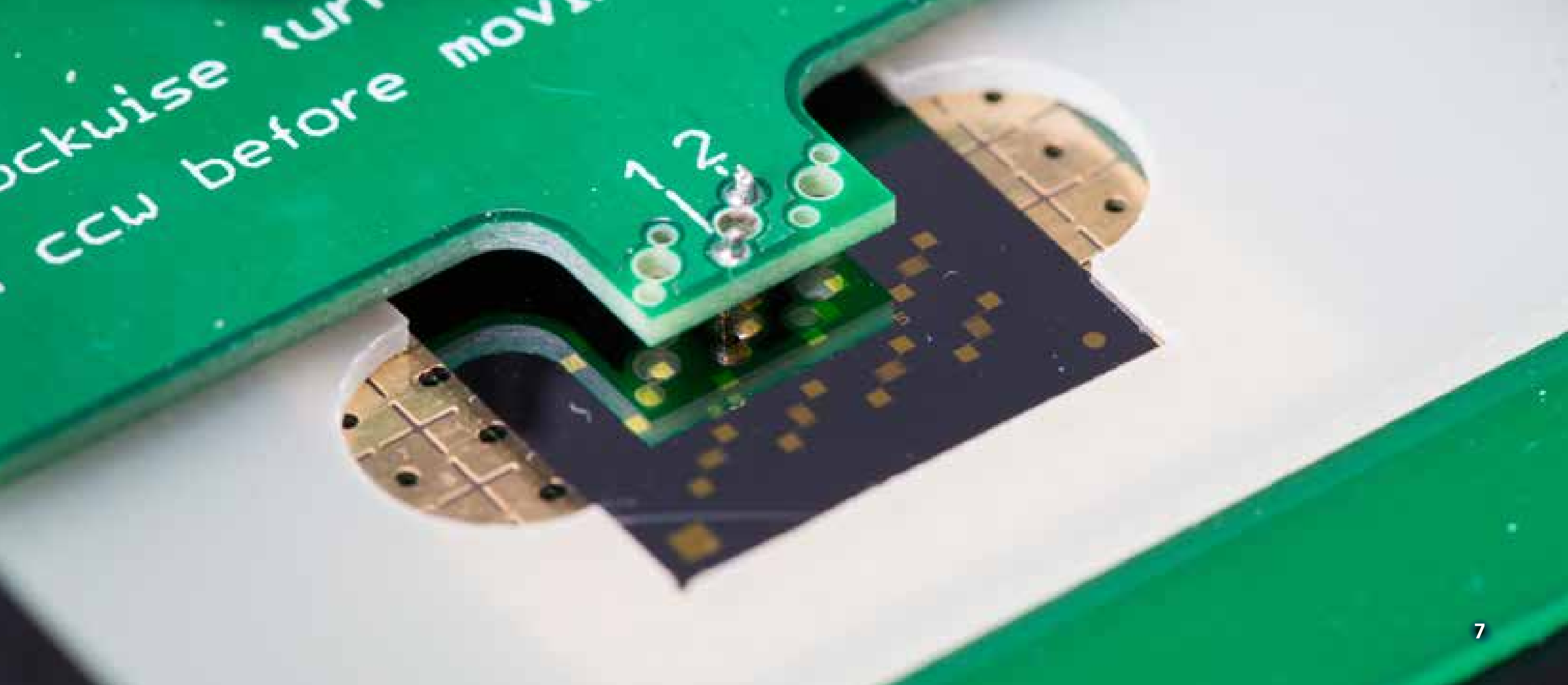


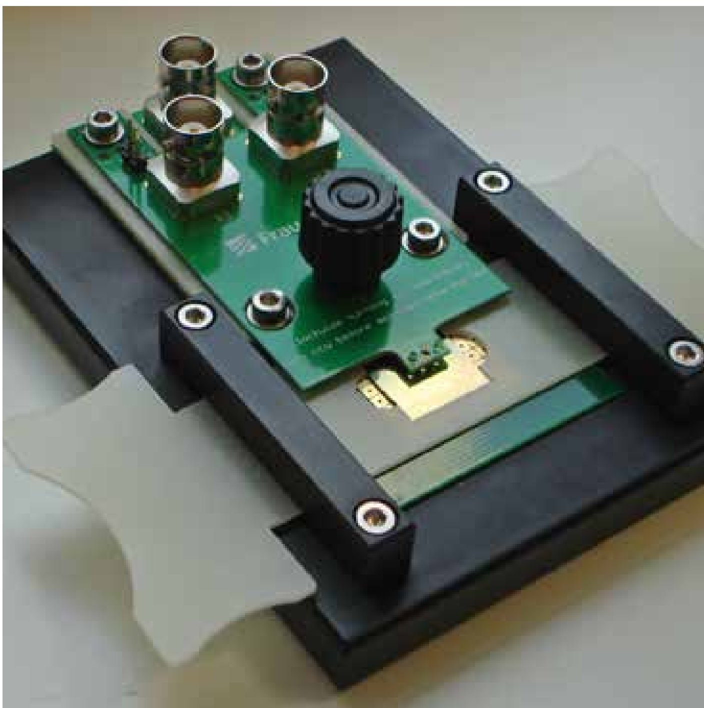


4 *LOFET Chips on Wafer*

5 *Layout of the Basic Logic Circuit with LOFET*

6 *LOFET Waferstack*





The OFET Miniprober

In order to simply and quickly measure OFET components with a given substrate size, pad grid and pad arrangement in large batches, Fraunhofer IPMS has developed a miniprober (Figure 8).

It has two electric connections on the front (source and drain) and one connection on the back (gate) and does not require probe station, samplers or manipulator pins.

A reliable interconnection is established on contact pads, which are only 0.5 × 0.5 mm² in size. Customized versions of the miniprober varying the connection arrangement, the position and number of the pads are possible. This makes the miniprober suitable for other applications in addition to OFETs. Signals are transmitted to the measurement instrument by BNC or triax cables.

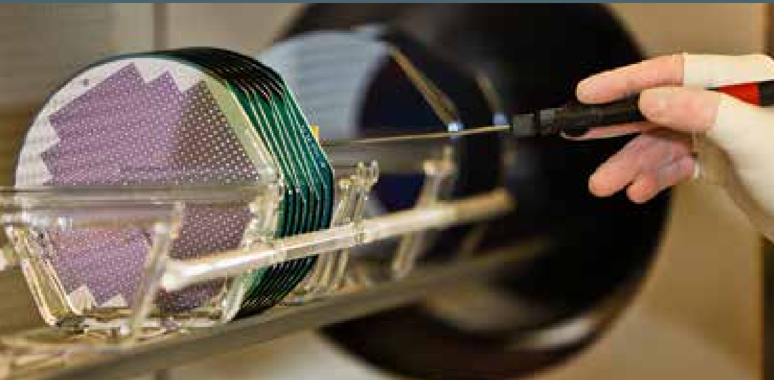
Advantages of the OFET Miniprober

- No probing system required
- Easy DUT handling
- Stable and secure connection
- Other chip sizes or pad arrangements possible
- Contact check with microscope recommended

7 *OFET Substrate Attached to Miniprober*
8 *OFET Miniprober*

Specifications

Parameter	Value
OFET	
Substrate (Gate)	n-doped silicon (doping at wafer surface: n~3·10^{17} cm^{-3}), 150 mm wafer according to SEMI standard (675 ± 20 µm thickness)
Gate Oxide	230 ± 10 nm SiO_2 (thermal oxidation) Other oxide thicknesses (90 … 500 nm) can be realized upon request
Contacts (Drain/Source)	30 nm Au with 10 nm high work function adhesion layer (ITO) (structured by lift-off technique)
Test Chip Size	15 × 15 mm²
Test Chip Transistor Configurations	**Gen. 4** / **Gen. 5** / **Customer Layout** 4 transistors L = 2.5 µm: W = 10 mm / W = 2 mm / available upon request 4 transistors L = 5 µm: W = 10 mm / W = 2 mm 4 transistors L = 10 µm: W = 10 mm / W = 2 mm 4 transistors L = 20 µm: W = 10 mm / W = 2 mm Contact pads 0.5 × 0.5 mm²
Shipment Type	Diced wafer (60 test chips at 15 × 15 mm²) on foil with air tight packaging Resist protection layer AZ7217 (soluble in AZ thinner or acetone)
OFET (trimmed)	
Substrate (Gate)	n-doped silicon (doping at wafer surface: n~3·10^{17} cm^{-3}), 150 mm wafer according to SEMI standard (675 ± 20 µm thickness)
Gate Oxide	230 ± 10 nm SiO_2 (thermal oxidation) Other thicknesses from 10 nm to 500 nm are available upon request
Test Chip Size	15 × 15 mm² (standard), other sizes are available upon request
Shipment Type	Diced wafer (60 test chips at 15 × 15 mm²) on foil with air tight packaging Resist protection layer AZ7217 (soluble in AZ thinner or acetone) Undiced wafer also available upon request
LOFET	
Wafer	150 mm according to SEMI standard
Structure Classes	11 transistors, 4 inverters and 4 ring oscillators; additional technology test structures
Die Size	15 × 15 mm²
Number of Dies	60
Number of Pads	39 + 2
Pad Size	1200 × 800 µm²
Gate Oxide	200 ± 10 nm
Structured Layers	3 (gate, contacts, drain/source)
Source/Drain Layer	Ti/TiN, Rs approx. 10 Ω/sq.
Contacts	Standard 20 × 20 µm², R approx. 20 Ω
Top Layer	70 nm Au with 10 nm high work adhesion layer (ITO, structured by lift-off technique) Rs approx. 0.65 Ω/sq. / 0.45 Ω/sq.
Shadow Mask	possible, but not required
Probecard	possible, but not required
Shipment Type	Diced wafer (60 test chips) on foil with air tight packaging Resist protection layer AZ7217 (soluble in AZ thinner or acetone)
OFET Miniprober	
Size	120 mm × 110 mm × 35 mm
Wight	280 g
Material	Body: Aluminium, PCB: FR4
Contacts	Top side: spring contacts, gold plated, 0.33 mm diameter; Back side: FR4, gold plated
Connector	3 × BNC, Triaxial upon request
Functionality	Up-down movement of a thread and adjusting knob Warning! Do not use with hazardous voltages (>100V)



About Fraunhofer IPMS

The Fraunhofer Institute for Photonic Microsystems IPMS and its 280 employees turn over an annual research volume of 31 million euros. Direct commissions from industry contribute more than 50 percent to the annual budget, the rest is covered by publicly financed projects in applied research and basic funding.

One core competence of the institute comprises research, development, and pilot manufacturing of (optical) micro-electro-mechanical systems [MEMS, MOEMS] and wireless microsystems. Work at Fraunhofer IPMS is based on extensive scientific know-how, long-term application experience as well as modern equipment. The latter includes a 1500 m² (15,000 ft²) class 10 clean room (ISO Class 4) equipped with state-of-the-art tools. Its infrastructure as well as the three-shift work organization follow latest industry standards. The clean room facilities and processes are certified for the development and fabrication of microsystems according to ISO 9001:2008. It allows flexible manufacturing concepts and is already configured for the demands of future machine generations.

Additionally, Fraunhofer IPMS works in the field of nano and micro electronics with functional electronic materials, processes and systems, device and integration, mask-less lithography and analytics. Another 800 m² of clean room space (clean room class 1000) is available for this purpose, along with analysis and metrology processes with atomic resolution and high sensitivity.

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