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Quasi-Monolithic Integration (QMI) Enables New Possibilities for Sensor and MEMS Applications

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A major component of APECS is the development of quasi-monolithic integration (QMI). In today's world, where technological advances are happening at breakneck speed, it is essential that the integration of different technologies is also at the highest level. This is where quasi-monolithic integration comes into play - a groundbreaking method that breaks down the boundaries between back-end and front-end in microelectronics.

What is QMI?

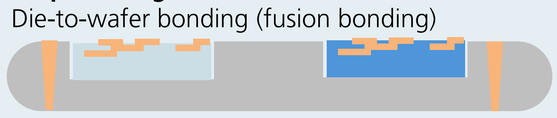
Quasi-monolithic integration refers to a technology in which different functional chiplets (CMOS, MEMS, non-silicon) are integrated into an almost monolithic system. In this technology, these integrated chiplets are arranged and connected with a common interconnect stack on an active or passive wafer substrate and then contacted within the front-end line. This allows the highest contact densities to be achieved. This maximizes the benefits of each technology while minimizing the challenges of integration.

Process flow for quasi-monolithic integration

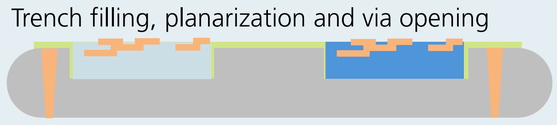
1. **Preparation of the wafer**
   Pocket and TSV fabrication

2. **Preparation of the chiplets**
   Dicing, backside grinding and polishing

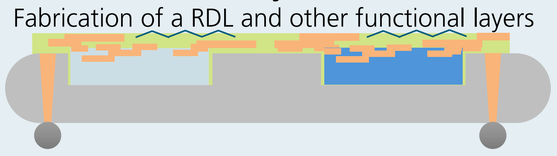
3. **Chiplet integration**
   Die-to-wafer bonding (fusion bonding)



4. **Passivation**
   Trench filling, planarization and via opening



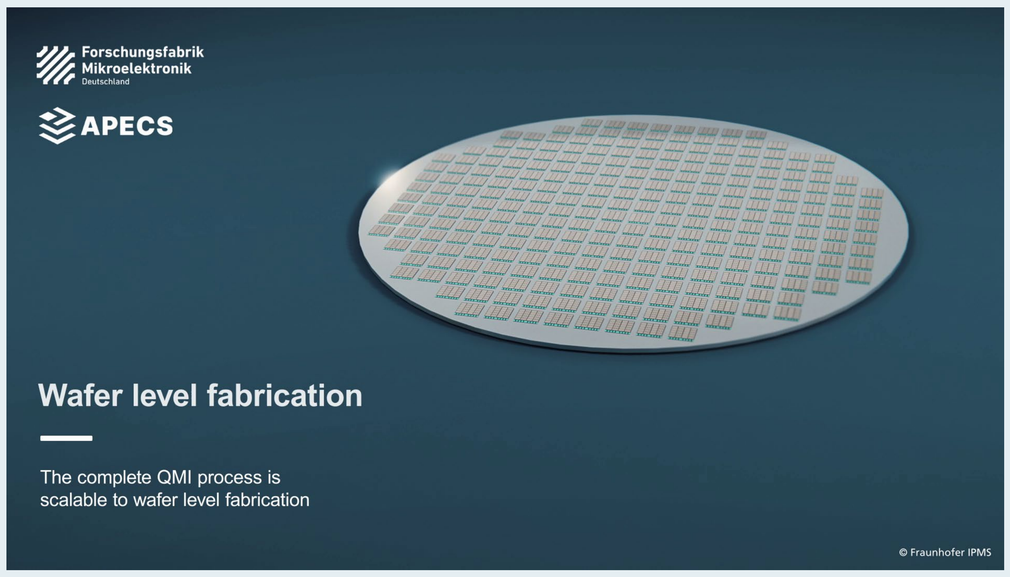
5. **RDL and functional layers**
   Fabrication of a RDL and other functional layers



Advantages of QMI

1. **Performance:** The tight integration of different elements significantly increases the performance of the system. Signal losses and delays are minimized, resulting in faster and more efficient data processing.
2. **Reliability and durability:** QMI systems are characterized by increased reliability and longer service life, as mechanical failures are reduced due to the tight connection of the components.
3. **Compactness:** QMI saves considerable space as the elements are integrated almost monolithically.
4. **Cost efficiency:** The combination of chiplets enables cost-efficient maximum integration with fast innovation cycles.

These advantages predestine quasi-monolithic integration for innovations such as highly integrated SOC (systems-on-chip) for AI applications (sensor AI) as well as intelligent transceivers with high bandwidth.



Animation explaining QMI.
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3D printed demonstrator
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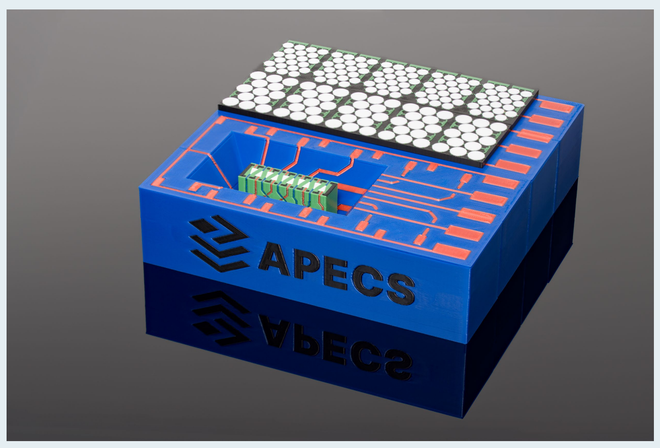
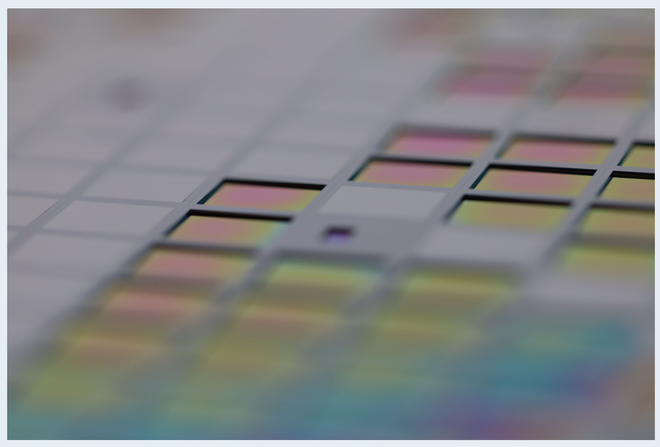


Results of the process developments



Pocket wafer with placed chiplets

Fully populated pocket wafer after the passivation step (CVD)

Fraunhofer IPMS plays a crucial role in the APECS pilot line and will drive the project's goals in chiplet development and integration technology. One part deals with the design of the chiplet system, where we build innovative system architectures for computing, artificial intelligence and MEMS sensors/actuators. The second major part covers new chiplet integration technologies on 200 and 300 mm wafers, including 3D stacking and 2.5D wafer-level integration, ultra-high density functional interposers and CMOS and MEMS/non-silicon chiplets. A major part of our contribution is the development of quasi-monolithic integration (QMI), which will set new standards in chiplet integration technology. Research in the areas of characterization, testing and reliability round off our research portfolio.

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Additional information

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