Fraunhofer IPMS

2.5D and 3D chiplet integration

2.5 and 3D integration technologies are crucial for creating powerful, compact and energy-efficient systems. Fraunhofer IPMS is developing technologies for 2.5D and 3D integration at 300 mm wafer level in close cooperation with Fraunhofer IZM-ASSID. The aim is to enable 3D stacking of advanced CMOS wafers and non-CMOS heterogeneous/multi-material wafers. In 2.5D integration, chiplets are to be integrated directly onto interposers. These developments are particularly important for applications in the fields of neuromorphic computing, trusted electronics (e.g. security functions) and are the basis for integrated high-performance chips.

Our research topics

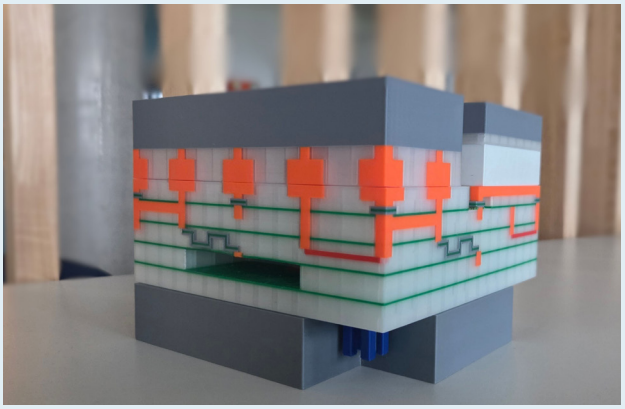
- Ultra-high-density (UHD) interposers
- Passive functionalized interposers
- 3D stack integration

The exhibit

The 3D model shows a silicon interposer with embedded passive functionalities connecting two demonstrator chiplets. TSV integration in the interposer substrate material offers connection possibility for high I/O density mounting on a substrate.

Capacitors and resistors are embedded between copper layers of the interposer and in the silicon substrate. Integrating passive devices in the interposer saves valuable space for active chiplets and significantly reduces the wiring distance between e.g. capacitors and active devices. Embedding 3D structures in the silicon substrate of the interposer offers room for high aspect ratio structures e.g. increasing capacitance.

The shown demonstrator chiplets are connected by hybrid bonding or copper µpillar technology. Both options are generally available in the APECS pilot line. Tradeoff between increased I/O density (hybrid bonding) and decreased process complexity/cost (µpillar) has to be taken into account for specific use cases.



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