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16 bit Microcontroller Core IPMS_430

The power-saving microcontroller family MSP430 of Texas Instruments belongs to the often-used microcontrollers worldwide. This microcontroller is particularly suitable for use in portable battery-operated systems because of the excellent qualities of the 16 bit CPU and the periphery modules. This microcontroller combines in a unique way system characteristics like computing power, memory resources and peripheral functions. A variety of software solutions for widely varying problems is available for this microcontroller family. For use in application-specific circuit design the Fraunhofer Institute for Photonic Microsystems developed a hardware description of the MSP430 CPU core. With this hardware description it is possible to transform system solutions based on the MSP430 microcontroller family into an application-specific circuit. The synthesizable microcontroller core IPMS_430 was developed in the hardware description language VHDL and is compatible in its properties, like instruction set, address space and time behavior with the standard CPU. Existing software programs behave without changes on this CPU core in the same manner. During the modeling of the CPU core properties were incorporated which permit a problem-oriented customization. To save valuable chip area unused CPU components like the interrupt system or unused internal registers can be omitted, the address space can be reduced and instructions not required by the software program can be removed.

It is also possible to attach periphery components of the model family or self-developed extensions to the CPU core. The CPU has a Neumann architecture, this means that storage components like RAM and ROM as well as all periphery components are in a common address space with a maximum size of 64K bytes. The CPU core has sixteen 16 bit registers at its disposal, therefrom 12 registers can arbitrarily be used as address or data registers. Additionally program counter, stack pointer and so-called constant registers are implemented. The status register contains information about the result of arithmetical or logical operations and is used for the control of the CPU. The instruction set supports 7 addressing modes for the source operand and 4 address modes for the target operand. The efficient RISC instruction set distinguishes 3 formats, instructions with 1 or 2 operands and branching instructions. The instruction set is further enlarged by emulated instructions, which can be combined in a suitable way from the 27 basic instructions. The interrupt system permits the interruption of the current program execution at programmed events of the periphery components.
You distinguish between maskable and non-maskable interrupt events. The realized interrupt system supports the definition of the priority for the individual interrupt sources. The combination of the interrupt event with the software routine is carried out via a jump distributor table in the main memory whose address is determined by the interrupt source.

The power consumption of the CPU core is reduced to the standby current by switching off the system clock.

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Table 1 shows the input and output signals of the VHDL description. Bidirectional signals were not used in this model.

The memory interface supports memory modules organized either in 8 bits or 16 bits by the separation of the address selection signal. Every read access by the CPU is announced with the activation of the address selection signals as well as the validity of the memory address. The module chosen by this address switches the corresponding data to the memory data input. If the data write signal is also activated, the selected module transfers the data from the memory data output into the corresponding internal storage position. This concept was chosen to use different modules in the address space.

The interrupt inputs show the CPU the request of an interrupt by a periphery module. The priorization of the interrupt request is achieved by a serial connection of several modules. If the CPU accepts the interrupt signal it activates the request signal for the interrupt vector and switches the 5 low-order bits of the address bus to high impedance.

The corresponding periphery module completes these 5 bits of the memory address for reading the assigned interrupt vectors. At the same time this request signal is used to acknowledge the interrupt request.

Name	D	Function
mab	O	memory address bus
mdb_o	O	memory data output
mdb_i	I	memory data input
mdbcsl_n	O	address selection low-order byte
mdbcsh_n	O	address selection high-order byte
mdbwr_n	O	write data signal
nmirq	I	non-maskable interrupt
gmirq	I	maskable interrupt
irqa	O	request interrupt vector
mclk	I	CPU system clock
puc_n	I	CPU system reset

1 *Input and output signals of the VHDL description.*

The developed synthesizable hardware description of the MSP430 CPU was verified in a 0.5 µm standard CMOS technology. The description on hand is also suitable for the implementation of the CPU in a FPGA and was tested practically with an Altera Flex10k. An efficient 16 bit RISC CPU for use in application-specific circuits or systems with FPGA realizations is available with this CPU modeling. The implemented configuration properties permit an adaptation of the properties to the system requirements to reach area or performance savings.

Also, developed periphery modules of the example microcontroller stand at disposal.

Features

- 16 bit RISC CPU
- 64 Kbytes addressable storage
- 7 address modes for source operands
- 4 address modes for target operands
- 27 base instructions
- interrupt system with priorization
- no limitation of interrupt or subroutine depth
- twelve 16 bit CPU registers
- power-down mode

Application areas

- microcontroller for application-specific circuit design
- FPGA systems with microcontroller
- a substitute or expansion of MSP430 based systems by full integration of the components

Characteristics

- synthesizable VHDL description
- instruction set and behavior based on the model of CPU
- configurable CPU properties
- general memory interface
- existing software utilizable without changes with the same behavior
- required area 0.5 µm CMOS
  3820 gate equivalents
  25 MHz system clock frequency
- required area Flex10k
  376 flipflops
  1334 logic cells
  8 MHz system clock frequency