AUTOMOTIVE IP CORES

Fraunhofer IPMS offers various IP core designs for on-board networking of vehicles. The automotive IP designs are developed platform-independent and are suitable for integration in FPGAs as well as in ASICs. The many years of experience can be seen in more than 150 users worldwide - the majority of the IP cores are used in vehicles.

FUNCTIONAL SAFETY - ISO 26262

Functional safety is an essential prerequisite for safety-critical systems that are used in vehicles, for example in ADAS SoCs and modules. Specific ASILs (Automotive Safety and Integrity Levels) must be met for each application. Compliance with the standard also applies to the IP that is integrated into the SoC. The IPMS develops automotive IP designs with functional safety in mind and makes it easier for manufacturers to achieve the ASIL levels for vehicle safety of their products, which are classified in the ISO 26262 standard for vehicle safety.

TURNKEY SOLUTIONS

Fraunhofer IPMS provides you with comprehensive advice on all issues relating to FPGA development and adapts and develops IP cores and SoCs according to your requirements. The multidisciplinary IP design team at Fraunhofer IPMS with specialist knowledge of domain-specific computer architectures, RTL design and the implementation of electronic systems is at your disposal as a competent development partner at every stage of development.

CAN IP CORE

The IP core carries out serial communication in accordance with the CAN 2.0, CAN FD and CAN XL specification. It is certified as ASIL-B-ready according to ISO 26262 for functional safety. Further ASILs can also be implemented on request.

LIN IP CORE

The UN IP Core enables components with a LIN interface to be implemented and supports the LIN specification 2.0, 2.1 or 2.2. The LIN IP core can be integrated into ASICs and FPGAs.

Ethernet TSN IP Cores

Fraunhofer IPMS develops Time Sensitive Networking IP Cores for deterministic and time-synchronized data transmission in Ethernet networks such as end point, switched end point and switch. The IP cores are designed for ASICS technologies or can be integrated into FPGA designs.

LOW LATENCY ETHERNET MAC CORE

The IP core implements an Ethernet Media Access Controller (MAC) that is compatible with the IEEE 802.3 and IEEE 802.3-2002 specifications at 10/100 Mbps and 1Gbps. It has extremely low input and output latency.

SHORT PROFILE

Fraunhofer IPMS is a worldwide leader in research and development services for electronic and photonic micro-systems. For more than 10 years, Fraunhofer IPMS provides industrial communication controllers as IP cores for ASIC and FPGA systems, as well as customer-specific adaptations, implementation support and characterization. Our strict customer orientation is essential to us and underscored with our ISO 9001 certification. Fraunhofer IPMS is part of Silicon Saxony, the largest microelectronics network in Europe.