



TSN-SE | ETHERNET TSN SWITCHED ENDPOINT CORE

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Overview

Time-Sensitive Networking (TSN) is a set of sub-standards that enhance the existing Ethernet specification towards time synchronization and deterministic communication in switched networks according to existing IEEE 802.1 and 802.3 standards. The goal is it to make Ethernet more suitable for the advancing needs of industrial and automotive applications. The TSN Ethernet IP core TSN-SE provides TSN switched endpoint functionality and eases the integration of devices into networks complying with the TSN standards. Two external 10/100/1000 Mbps ports are available beside an internal CPU port. The design implements a 1GbE switching bar with cut-through capability. It provides time-sensitive networking for full-duplex point-to-point Ethernet communication enabling daisy chaining of devices or ring architectures. The IP core consists of two instances of the TSN-EP IP and a switching bar as well as additional

routing logic optimized for low latency communication.

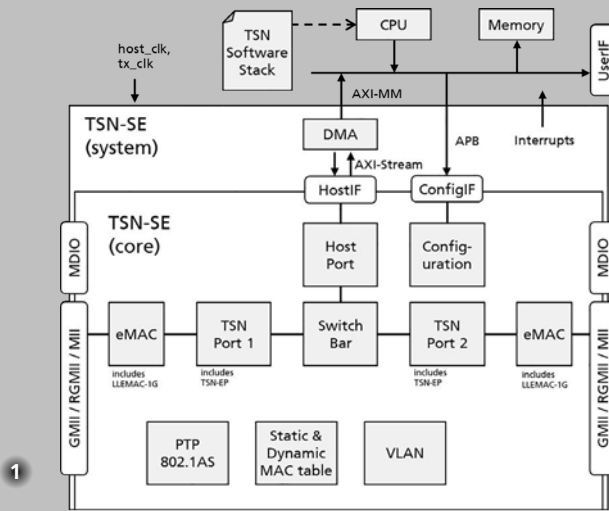
Applications

The TSN-SE IP Core is suitable for the implementation of talkers and listeners within TSN Ethernet networks. The TSN-SE IP can be utilized for embedding real-time TSN applications into regular Ethernet networks. It is targeting for applications in industrial automation, robotics, automotive, aerospace and more.

Verification

Interoperability and conformance of sub-modules is constantly tested within TSN plug-fests by LNI 4.0 and Industrial Internet Consortium (IIC).





TSN Features

- IEEE 802.1AS
- IEEE802.1Qav
- IEEE802.1Qbv
- IEEE802.1Qbu / IEEE 802.3br
- Coming in 2020: IEEE802.1AS-2020, IEEE 802.1CB, IEEE, 802.1Qci, IEEE 802.1Qcc, IEEE, 802.1Qch)

IEEE 802.1Q Switch Features

- Layer 2 switch cut-through architecture
- 2 Gigabit TSN ports and 1 host port
- Supports up to 1024 dynamic and 1024 static MAC table entries
- Supports IEEE 802.1Q VLAN-tags with up to 1024 entries
- Cut-through or store-and-forward TSN frame forwarding
- Ports run full-duplex at 10/100/1000 Ethernet
- PHY configuration via MDIO

Designed for usage with Ethernet MACs

- ALTERA/Intel Triple Speed Ethernet MAC
- XILINX Tri-Mode Ethernet MAC
- IPMS Triple Speed Low-Latency Ethernet MAC
- Triple speed: 10 / 100 / 1000 Mbit/s Ethernet
- PHY Interfaces to MII, GMII and RGMII
- Ingress latency: 6 Rx clock cycles
- Egress latency: 10 Tx clock cycles

Easy Integration

- TSN-SE IP core can be attached to custom SoC or a complete TSN-SE can be provided
- Intel Altera based evaluation platform
- Xilinx based evaluation platform
- Set of demo projects for Xilinx and Altera
- Configurable feature set
- Responsive support

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Test benches
- Sample simulation and synthesis scripts
- Comprehensive documentation
- PTP software stack in plain C as source code or precompiled library
- FreeRTOS example projects
- Linux driver and example implementation

Data Interfaces

- Advanced Peripheral Bus (APB) for memory mapped register access
- 2 – 8 AXI-Streams for TX data (configurable byte width)
- 1 AXI-Stream for RX data (configurable byte width)
- Avalon interfaces available
- More interfaces upon request