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TSN-EP | ETHERNET TSN ENDPOINT CORE

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Overview

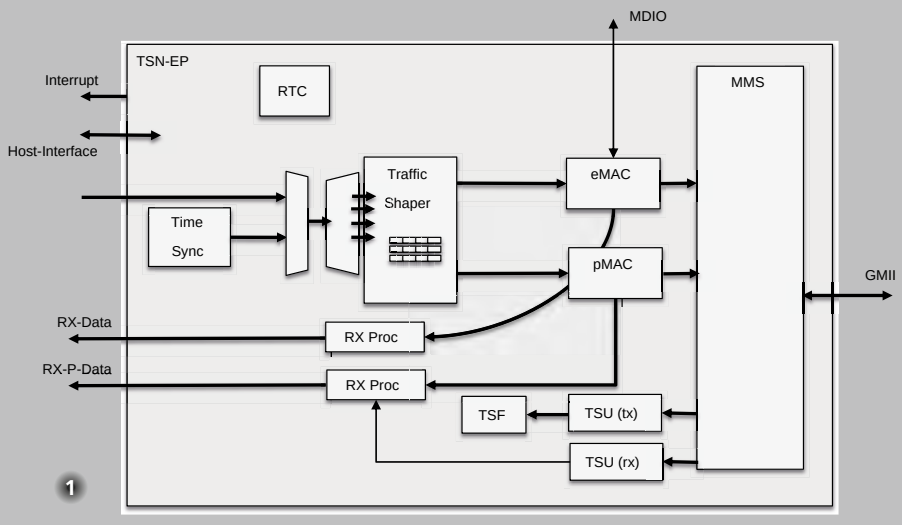
Time-Sensitive Networking (TSN) enhances the Ethernet specification towards time synchronization and deterministic communication (specifically IEEE 802.1 and 802.3). The goal is it to make Ethernet more suitable for the advancing needs of industrial and automotive applications.
The TSN Ethernet IP core TSN-EP eases the integration of devices into networks complying with the TSN standards. It provides time-sensitive networking for full duplex point-to-point Ethernet communication. The IP core consists of three sub-modules for time synchronization, traffic shaping and low latency Ethernet MAC communication.

Applications

The TSN-EP IP Core is suitable for the implementation of talkers and listeners within TSN Ethernet networks requiring time synchronization as well as robust, low-latency, and deterministic communication. It is targeting for applications in industrial automation, robotics, automotive and more.

Verification

Interoperability of sub-modules tested within TSN plug-fests by LNI 4.0 and Industrial Internet Consortium (IIC).



TSN Features

- IEEE 802.1AS
- IEEE802.1Qav
- IEEE802.1Qbv
- IEEE802.1Qbu / IEEE 802.3br
- Coming within 2020 (IEEE 802.1AS-2020, IEEE 802.1CB, IEEE, 802.1Qci, IEEE 802.1Qcc, IEEE 802.1Qch)
- Specialized DMA-core on request

Interfaces

- Advanced Peripheral Bus (APB) for memory mapped register access
- 2 - 8 AXI-Streams for TX data (configurable byte width)
- 1 AXI-Stream for RX data (configurable byte width)
- Avalon interfaces available
- PHY: MII, GMII, RGMII

Designed for usage with Ethernet MACs

- ALTERA/Intel Triple Speed Ethernet MAC
- XILINX Tri-Mode Ethernet MAC
- IPMS Triple Speed Low-Latency Ethernet MAC
- Triple speed: 10 / 100 / 1000 Mbit/s Ethernet

Easy Integration

- Intel Altera based evaluation platform
- Xilinx based evaluation platform
- Set of demo projects for Xilinx
- Altera configurable featureset
- Optimized for multiport bridging operation
- ASIC & FPGA design support

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Test benches
- Sample simulation and synthesis scripts
- Comprehensive documentation
- PTP software stack in plain C as source code or precompiled library
- FreeRTOS example projects
- Linux driver and example

1 *Schematic diagram of the TSN-EP*