

1 LIN core pinout.

LIN CONTROLLER CORE – IPMS_LIN

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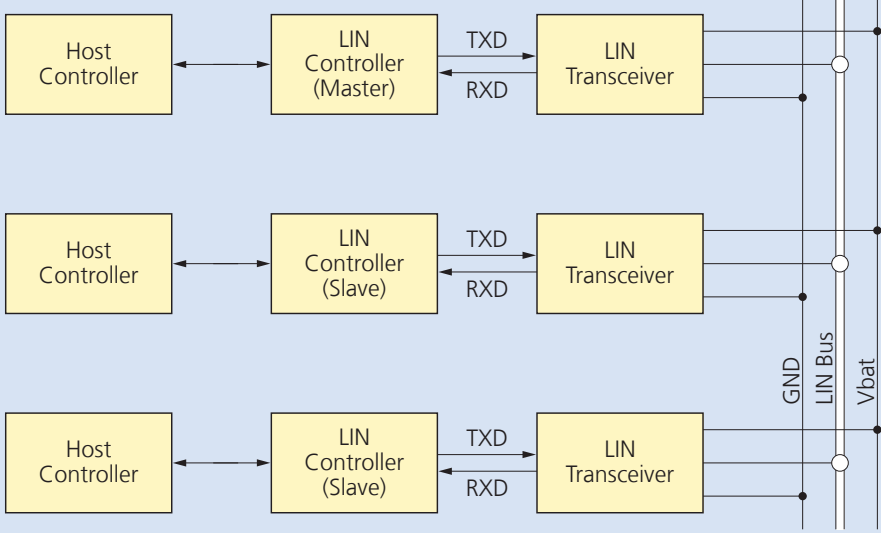
LIN (Local Interconnect Network) is a serial communication protocol used in low cost automotive networks. It enables cost efficient bus communication for applications where the bandwidth of CAN is not required.

The IPMS_LIN Core enables the customer to realize components with LIN interface. It is described as fully synchronous VHDL model that can be synthesized to a netlist by using a standard cell library or a FPGA.

The VHDL model has been implemented and successfully tested with a Xilinx Virtex II FPGA.

The IPMS_LIN Core supports LIN specification 2.0. It comprises an 8-byte data buffer and an 8-bit host controller interface. Fig. 1 shows the LIN core pinout and fig. 2 shows the description of the control signals.

A LIN message frame comprises from zero to eight data fields. The LIN controller core transmits or receives complete frames (with all data fields). Therefore, no interrupts to the host controller are requested until all data fields are transmitted.



2 LIN system with one master and two slaves.

Features

- Support of LIN specification 2.0
- Programmable data rate between 1 Kbit/s and 20 Kbit/s
- 4 MHz clock frequency
- 8-byte data buffer
- 8-bit host controller interface
- Support of master and slave functionality configurable by generics
- Slave can be implemented with or without clock synchronization
- Fully synchronous VHDL or Verilog design, completely synthesizable

Application

The VHDL model can be translated to a netlist by using an available standard cell library or a FPGA. That enables the realization of a chip or FPGA design with LIN interface.

A LIN system comprises one Master node and several Slave nodes. The VHDL description supports master and slave functionality. Generics are used to configure whether the LIN core is implemented as master or as slave.

Fig. 3 shows the connection of LIN controller, host controller and transceiver IC for a LIN system with 3 nodes.

Name	Type	Description
clock	I	system clock
rs	I	master reset (asynchronous)
ad	I	4-bit address from host
cs	I	chip select
we	I	write enable
oe	I	output enable
di	I	8-bit data from host
rx	I	receive data from bus
do	O	8-bit data to host
int	O	interrupt request to host
tx	O	transmit data to bus

3 Description of the LIN core signals.