

Chemical-mechanical planarization (CMP)

300 mm CMP tool

The CMP process

Highly integrated circuits, like logic and memory chips, consist of many material layers. In the course of manufacturing the surfaces have to be planarized over and over again to obtain sufficient process windows for critical processes like lithography and etching. Furthermore planarization ensures defined sizes of the structures, thus in the end reliable functioning of the electronic elements.

Chemical-mechanical planarization (CMP) is the state of the art to reach the necessary planarity. The continuous shrinking in the semiconductor technology goes along with a higher demand for accuracy, as well as a higher number of materials used. Therefore it is necessary to understand the various CMP processes and to develop novel processes for newly introduced materials to be able to fulfill the demands of the coming technology nodes.

Advantages at CNT

- Industry matched 300 mm CMP system for efficient portability into large-scale production
- Extensive experience in the field of consumable screening and characterization
- Long-standing experience in process characterization and development
- Close location and cooperation with semiconductor manufacturers and research institutions in Silicon Saxony
- Established qualification and contamination protocols for customer demos and loop of production wafers
- Test wafer availability
- Extensive metrology and analytics
- Electrical characterization and reliability tests
- Pre and post processing in house (barrier/liner/seed deposition, copper ECD, anneal, etc.)
- ISO 9001 certified



MATERIAL
SUPPLIERS



IC
MANUFACTURERS



EQUIPMENT
MANUFACTURERS



BASIC RESEARCH
INSTITUTIONS

Contact

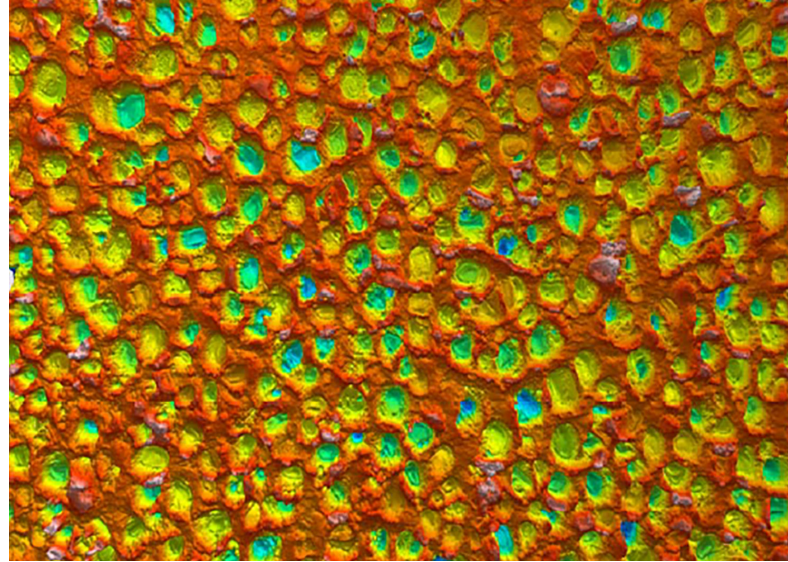
Dr. Conrad R. Guhl
+49 351 2607 3235
conrad.guhl@ipms.fraunhofer.de

Fraunhofer Institute for
Photonic Microsystems IPMS
Center Nanoelectronic Technologies
An der Bartlake 5
01109 Dresden, Germany

www.ipms.fraunhofer.de
www.screening-fab.com



300 mm CMP test wafer with pitch / density structures down to 28 nm node



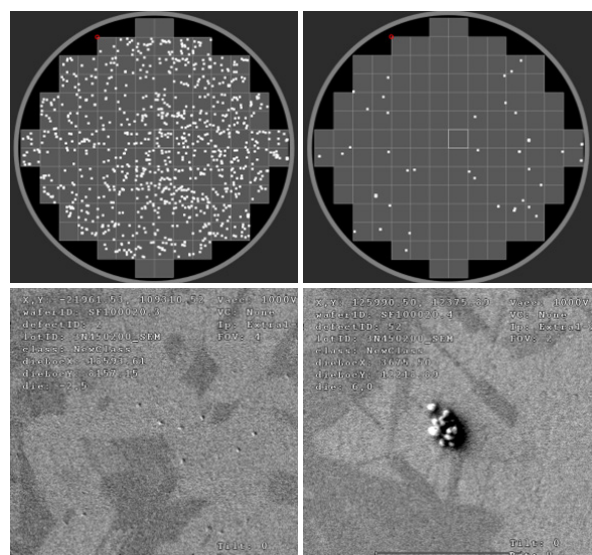
CMP pad pore structure obtained with confocal microscopy (0.7 x 0.5 mm)

Industry-matched equipment

- Applied Materials Reflexion LK polisher with Desica cleaner
- Flexible mobile slurry system (6 x 80 l)
 - 4 tanks for Platen distribution
 - 2 tanks for Cleaner feed
- Film thickness measurement tools
 - Ellipsometer (KLA Tencor Spectra CD/FX 100)
 - 4-Point-Prober (KLA Tencor RS-100)
- Surface topography measurements
 - Profiler (KLA Tencor HRP-340)
 - 300 mm confocal microscopy, white light interferometer (Nanofocus μcostom)
 - AFM (Park Systems NX-eAFM)
 - Mobile confocal microscope (Nanofocus μsurf)
- X-Section and material analyses:
 - SEM, TEM, ToFSIMS, TXRF, XRR, XRD, etc.
- Defect control
 - Blanket: KLA Tencor SP2 & SP3
 - Patterned wafer: NextIn AEGIS-I
 - Wafer surface potential measurements: Malvern Zetasizer Nano-ZS
 - Review: Applied Materials SEMVision G3E
- Slurry analysis
 - Particle & Zetapotential : (Malvern Zetasizer Nano-ZS)
 - surface tension (SITA DynTester+)
- Wafer availability
 - Unpatterned for removal rates and particle measurements: TEOS, ULK, Cu, Ta/TaN, Co, etc.
 - Patterned for defectivity and electrical data: test chips for STI & metallization processes in 2x nm node
- Simulation capabilities
 - Modeling on different scales, esp. feature and chip scale
 - In-house developed simulation programs and routines
 - FEM based commercial software COMSOL Multiphysics
- Electrical characterization
 - TEL Precio probe station (-55 – 200 °C, fully automated)
 - SÜSS PA300 probe station (semi-automated, flexible)

Applications

- CMP process development and optimization
- CMP design for manufacturing strategy development with semiconductor product manufacturers
- CMP consumables screening and characterization
 - Polishing pad
 - Conditioner
 - Slurry
 - Post CMP cleaning chemistry
 - Brush
 - Filter
- CMP process characterization
 - Planarization
 - Defectivity
 - Removal rates, selectivity
 - Static etch rates
 - Electrical performance and reliability
- Modeling and simulation of the planarization behavior of patterned wafers
- CMP wafer processing on demand



Defect maps on patterned 300 mm wafers with exemplary review SEM pictures