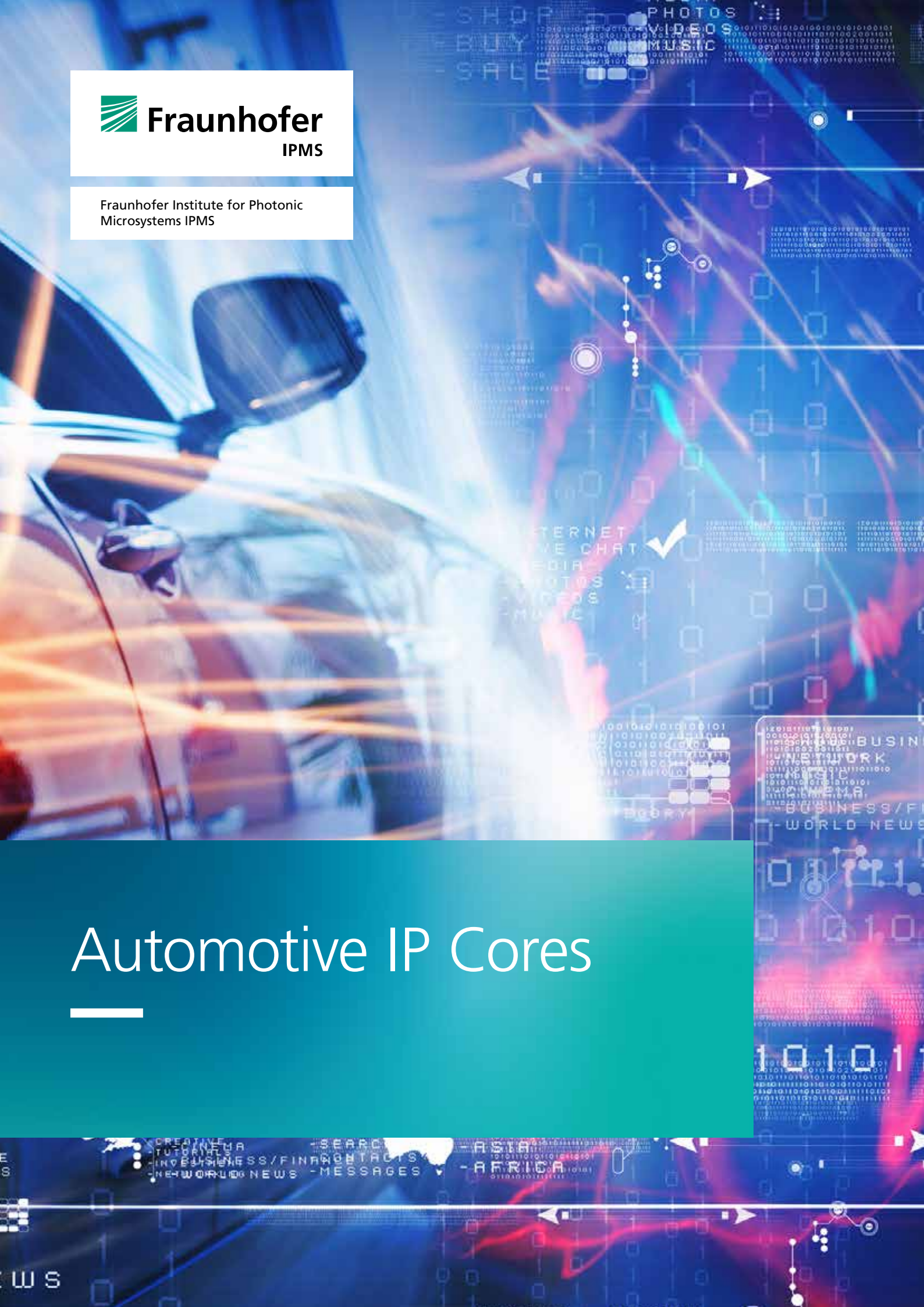
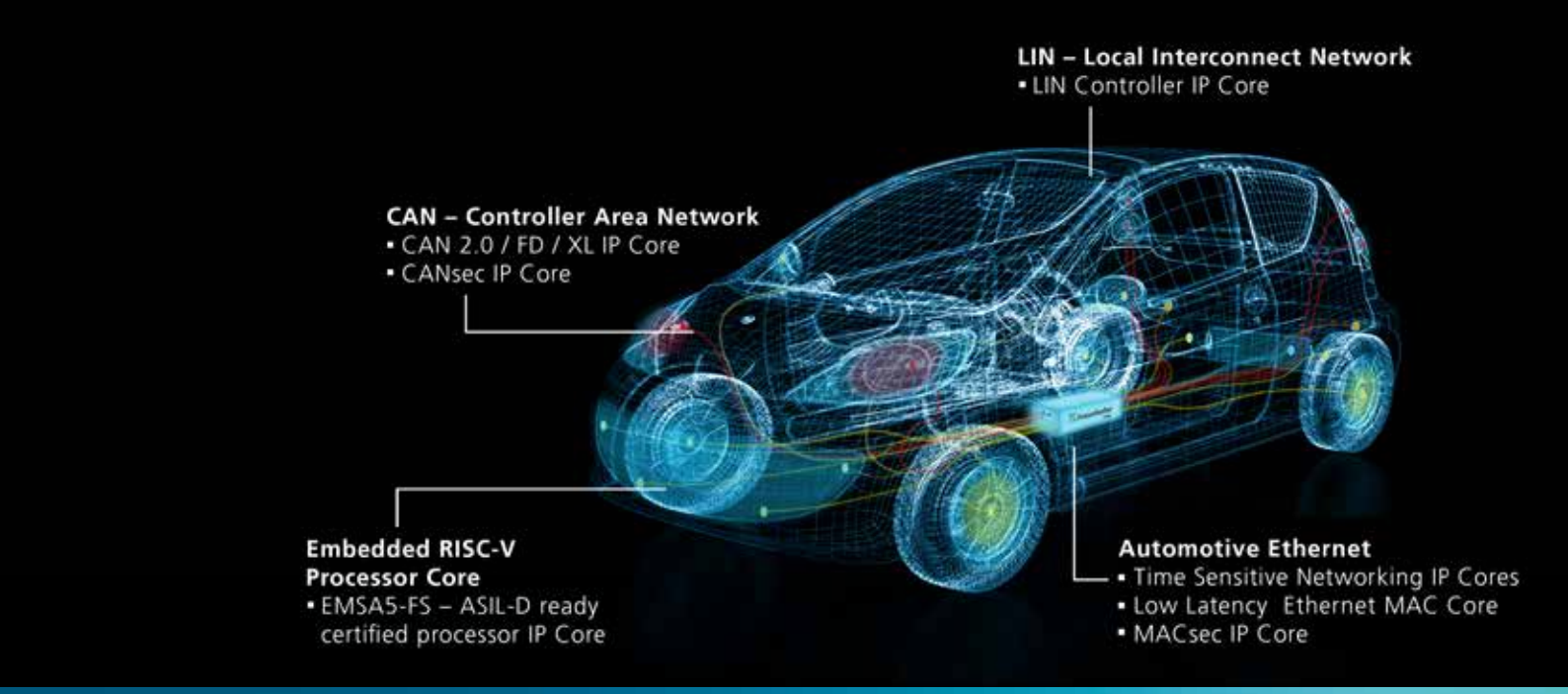


Fraunhofer IPMS

Fraunhofer Institute for Photonic Microsystems IPMS

Automotive IP Cores



Automotive IP Cores

Fraunhofer IPMS offers various IP core designs for on-board networking of vehicles. The automotive IP designs are developed platform-independent and are suitable for integration in FPGAs as well as in ASICs. The many years of experience can be seen in more than 150 users worldwide - the majority of the IP cores are used in vehicles.

Functional Safety – ISO 26262

Functional safety is an essential prerequisite for safetycritical systems that are used in vehicles, for example in ADAS SoCs and modules. Specific ASILs (Automotive Safety and Integrity Levels) must be met for each application. Compliance with the standard also applies to the IP that is integrated into the SoC. The IPMS develops automotive IP designs with functional safety in mind and makes it easier for manufacturers to achieve the ASIL levels for vehicle safety of their products, which are classified in the ISO 26262 standard for vehicle safety.

The requirements for the security of data transmitted within the vehicle grow equally with the complexity of the vehicle functions. Protective measures are necessary to ensure that information within the vehicle is transmitted completely and unchanged and that only authorized recipients have access to the data. For this purpose, IPMS develops automotive IP designs that extend the various automotive communication protocols by security functionalities such as authenticity, integrity and confidentiality.

Security for Vehicle Networks

The requirements for the security of data transmitted within the vehicle grow equally with the complexity of the vehicle functions. Protective measures are necessary to ensure that information within the vehicle is transmitted completely and unchanged and that only authorized recipients have access to the data. For this purpose, IPMS develops automotive IP designs that extend the various automotive communication protocols by security functionalities such as authenticity, integrity and confidentiality.

Turnkey solutions

Fraunhofer IPMS provides you with comprehensive advice on all issues relating to FPGA development and adapts and develops IP cores and SoCs according to your requirements. The multidisciplinary IP design team at Fraunhofer IPMS with specialist knowledge of domain-specific computer architectures, RTL design and the implementation of electronic systems is at your disposal as a competent development partner at every stage of development.

CAN Controller IP Core

The IP core carries out serial communication in accordance with the CAN 2.0, CAN FD and CAN XL specification. It is certified as ASIL-D-ready according to ISO 26262 for functional safety.

CANsec Controller IP Core

CANsec is an extension to the newly developed CAN XL protocol. It specifies a Layer 2 CAN security protocol that aims to protect the integrity and authenticity of the origin and confidentiality of data in CAN-based networks. The CANsec Controller IP Core can be used with the CAN-XL IP Core (CAN-CTRL) of Fraunhofer IPMS, with any other CAN IP Core or in standalone operations.

LIN IP Core

The LIN IP Core enables components with a LIN interface to be implemented and supports the LIN specification 2.0, 2.1 or 2.2. The LIN IP core can be integrated into ASICs and FPGAs. It is certified as ASIL-D-ready according to ISO 26262 for functional safety.

Ethernet TSN IP Cores

Fraunhofer IPMS develops Time Sensitive Networking IP Cores for deterministic and time-synchronized data transmission in Ethernet networks such as end point, switched endpoint and switch. The IP cores are designed for ASIC technologies or can be integrated into FPGA designs.

Low Latency Ethernet MAC Core

The IP core implements an Ethernet Media Access Controller (MAC) that is compatible with the IEEE 802.3 and IEEE 802.3-2002 specifications at 10/100 Mbps and 1Gbps. It has extremly low input and output latency. It is certified as ASIL-D-ready according to ISO 26262 for functional safety.

MACsec Controller IP Core

MACsec Controller IP Core is used for authentication and encryption of data packets between network devices. MACsec is a protocol for secure communication between trusted components within a LAN. It can be used with the LLEMAC core, any other Ethernet MAC IP core or in standalone operations.

Embedded RISCV Processor Core

Fraunhofer IPMS offers an IP Core processor based on the RISC-V architecture. The IP Core EMSA5 is available as a general purpose variant and as a safety variant with an ASIL-D ready certification according to ISO 26262: 2018 for functional safety and is therefore suitable for use in safety-critical systems in vehicles.

Competencies and Services

- Consulting
- Feasibility Studies
- Proof of Concept
- IP-Core Design
- Digital, Analog & Mixed-Signal Design
- Verification & Test
- Functional safety
- DFM
- System integration

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