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FUNCTIONAL FILMS FOR ON-CHIP LITHIUM-ION BATTERIES DEPOSITED BY ATOMIC LAYER DEPOSITION

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TOWARDS Li-CELLS ON-CHIP

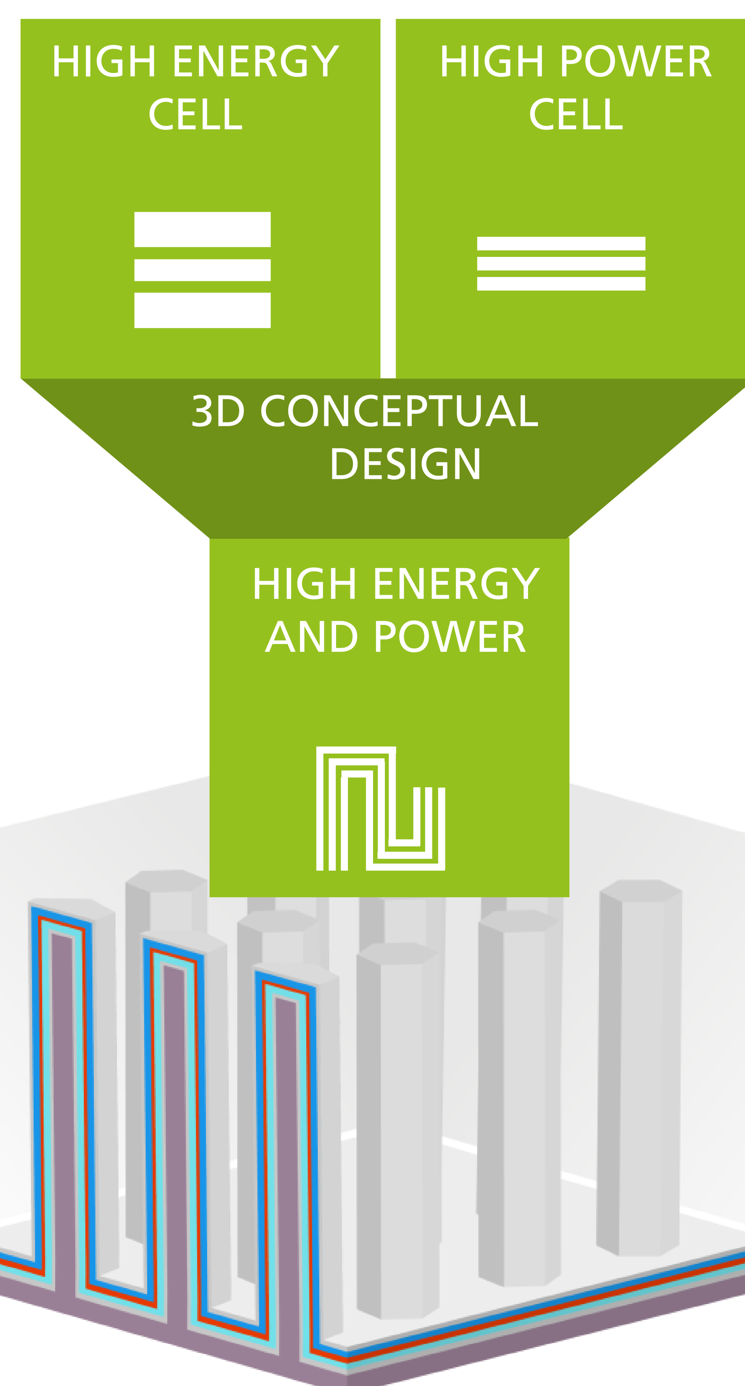
The technical transition to solid-state electrolytes means significant improvement of battery safety and even opens possibilities for integration into silicon technology.

Our aim is the development and characterization of functional layer stacks allowing for direct integration into microsystems.

For semiconductor compatible design and production we manufacture on silicon wafers using standard industrial thin film deposition equipment.

Fig. 1 *ALD electrolyte LiPON with protecting Al_2O_3 capping in trenches*

3D CELL DESIGN



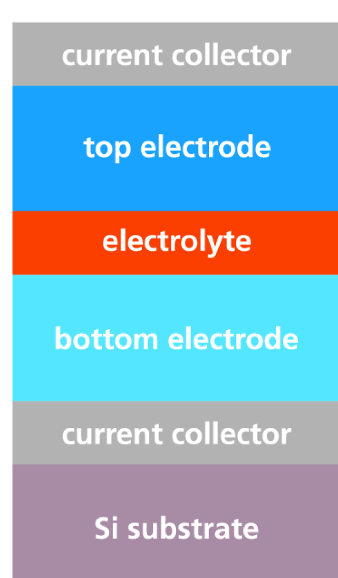


Fig. 2 *Schematic ALD-layer stack on 3D structured silicon substrate*

„BRING THE BATTERY INTO THE CLEAN ROOM"

- 800 m² clean room, class 1000 and 650 m² laboratory area
- 40 tools for wafer processing, patterning, metrology & analytics
- Qualification of processes & materials on 12 inch industrial standard equipment

- 8 inch silicon wafer, manual handling
- No universal Li-precursor
- Strict contamination management for clean room and analytics
- Excludes in-line metrology

Fig. 3 *(a) IPMS-CNT cleanroom (b) OXFORD Instruments FlexAL PEALD -Tool*

ALD PROCESS DEVELOPMENT ON SILICON SUBSTRATES

So far, our activities involve ALD process development, phase studies, physical, and electrochemical analysis on titanium oxide, lithium titanium oxide (LTO), and lithium phosphorous oxynitride (LiPON) to achieve satisfying functionality and wafer level uniformity.

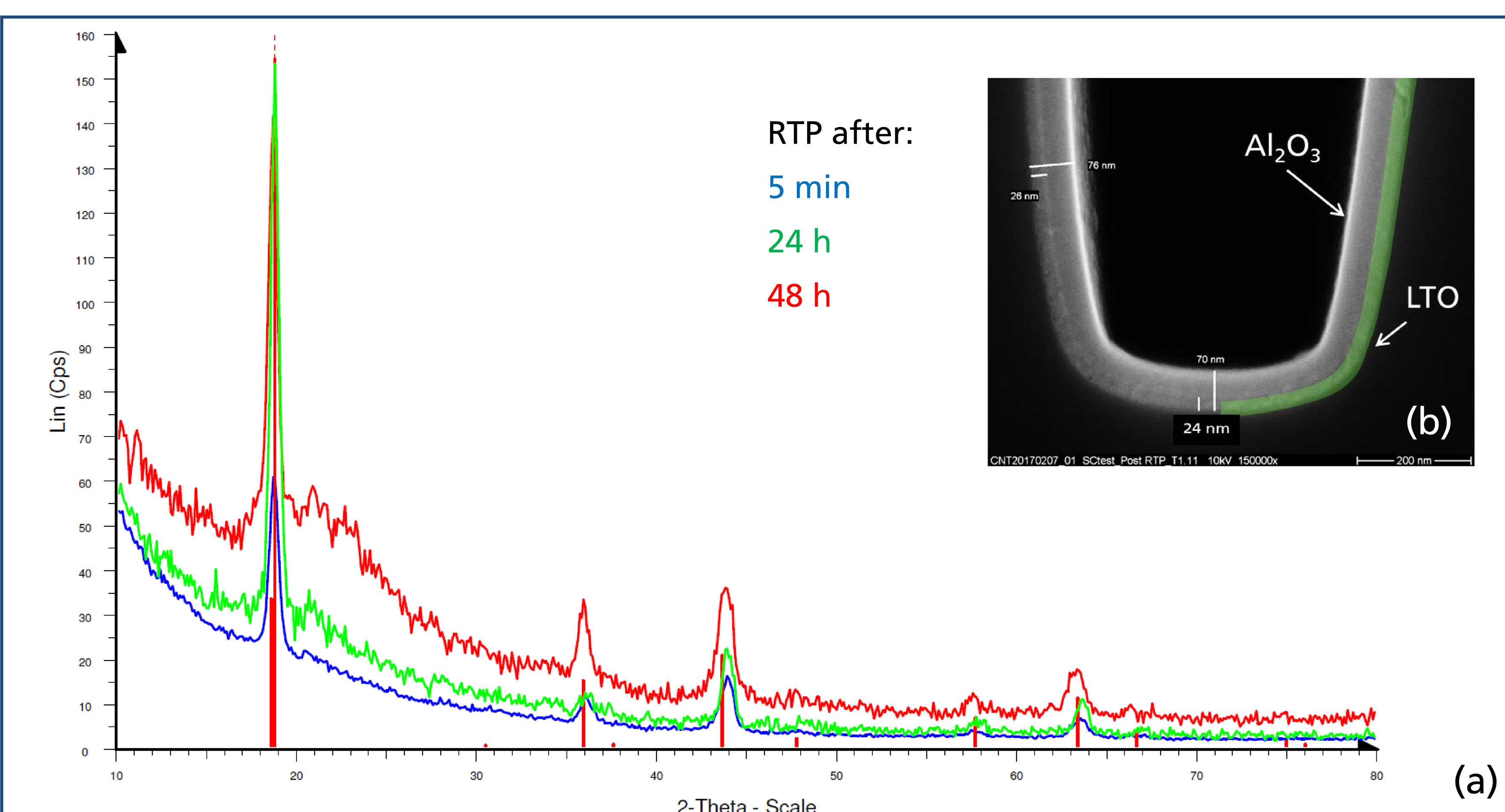


Fig. 4 *(a) Crystallized $Li_4Ti_5O_{12}$ films (~20 nm thick) by rapid thermal processing (RTP), red lines mark XRD reference pattern. Stability studies were performed 5 min, 24 h, and 48 h after deposition (b) SEM image, 3D LTO with capping*

LAYER STACK CHARACTERIZATION

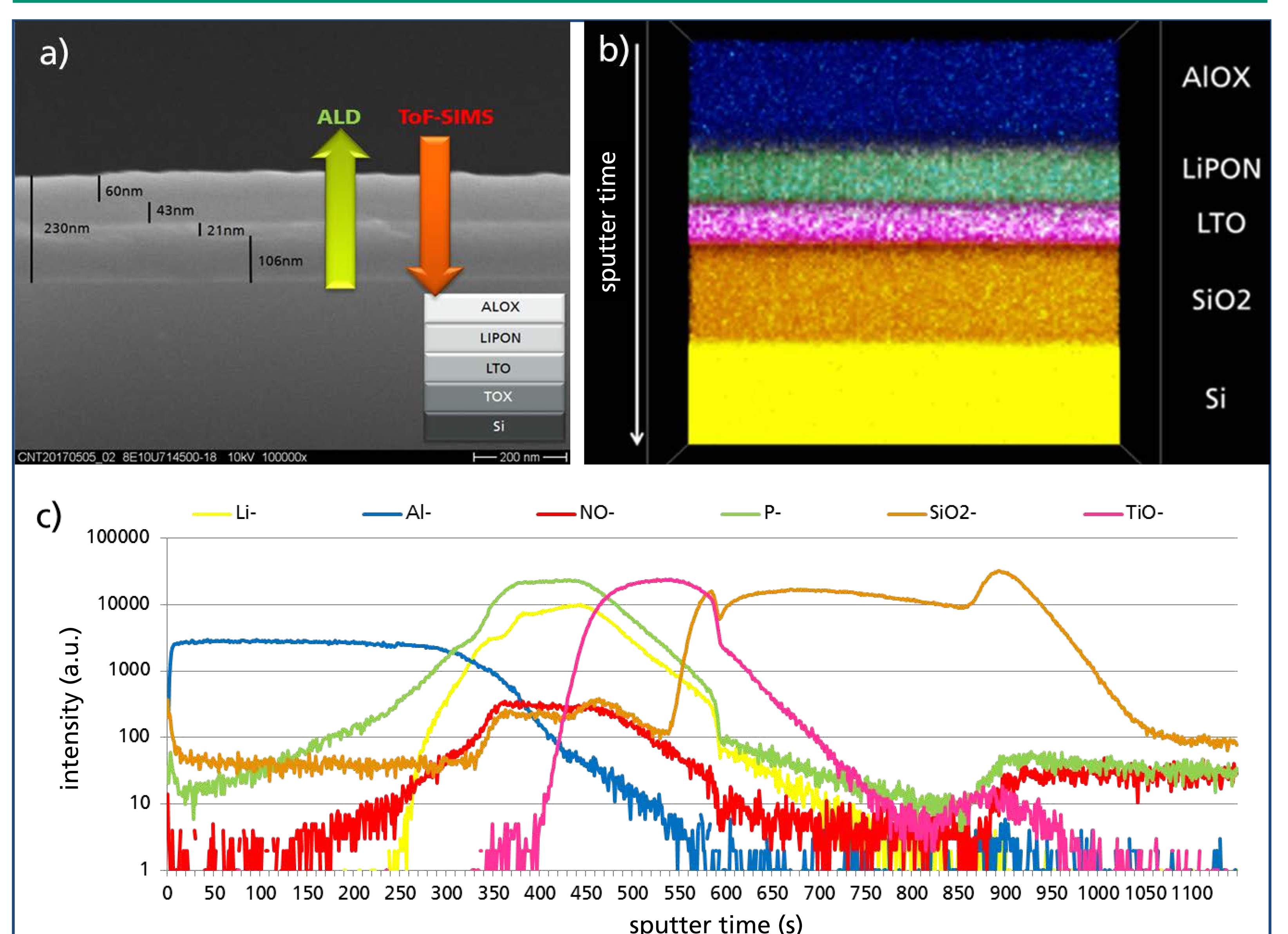


Fig. 5 *(a) SEM picture (b) and (c) ToF-SIMS element depth distribution*

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