

OFET measurement adapter 8T1G

Electrical characterization of materials

Measuring conductivity, contact resistance, and field effect is an established method for characterizing organic conductive and semiconducting materials and related materials. For this purpose, Fraunhofer IPMS offers test structures with interdigital electrodes as source-drain electrodes on a silicon chip. The doped bulk silicon of the chip can be used as a common gate electrode and is separated from the source and drain electrodes by a gate oxide.

The material to be examined can then be deposited using processes such as spin/spray/drop coating, dispensing, vacuum evaporation, inkjet, etc. Ideally, the contact pads are not coated to avoid contact problems. The coated chip can then be inserted

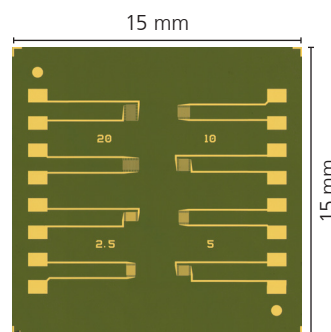
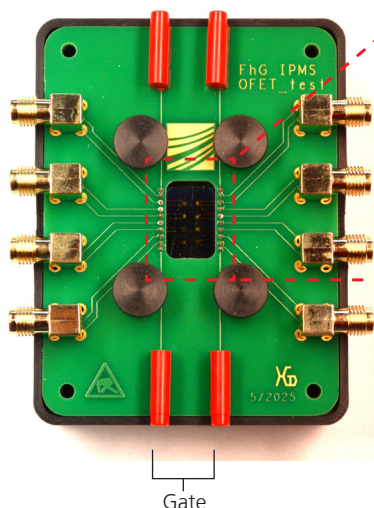
into the measuring adapter, and 4 source/drain pairs and the gate electrode are then contacted simultaneously and can be connected to the measuring setup via SMA connectors or banana plugs.

Since the active area of the chip is exposed, users can measure light or gas influences. If required, Fraunhofer IPMS can assist in the development of suitable, customer-specific extensions.

Currently, the AX1580 chip design is compatible with the adapter (see chip description and Figure 1). Depending on customer requirements, the chips can be supplied in a waffle pack or as a sawed wafer on a clamping frame. Of course, unsawn 200 mm wafers with 112 chips/wafer can also be supplied.

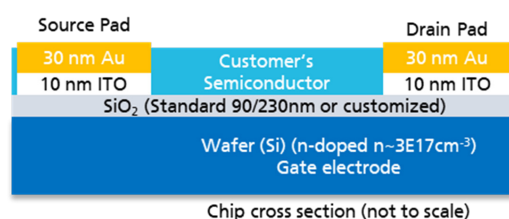
Source/Drain contact via SMA-connector

► **Figure 1:** OFET measurement adapter 8T1G for chip AX1580 (Fig. 2) for contacting 8 source/drain pairs with a common gate electrode

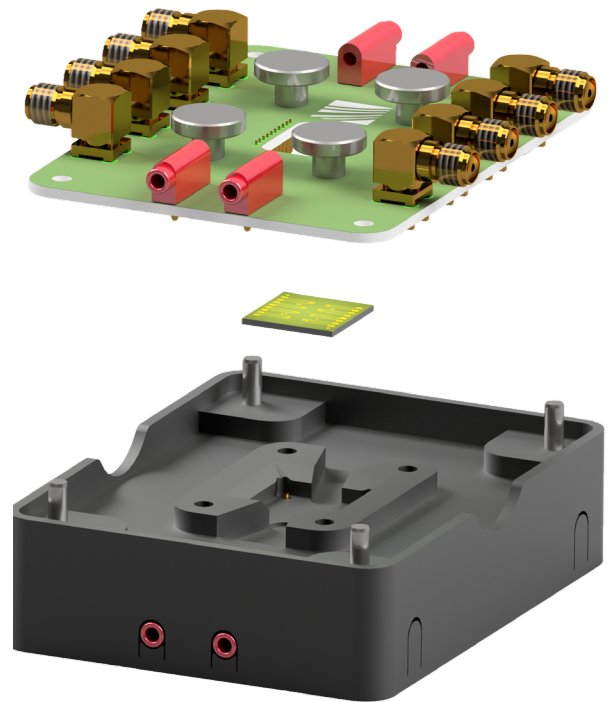
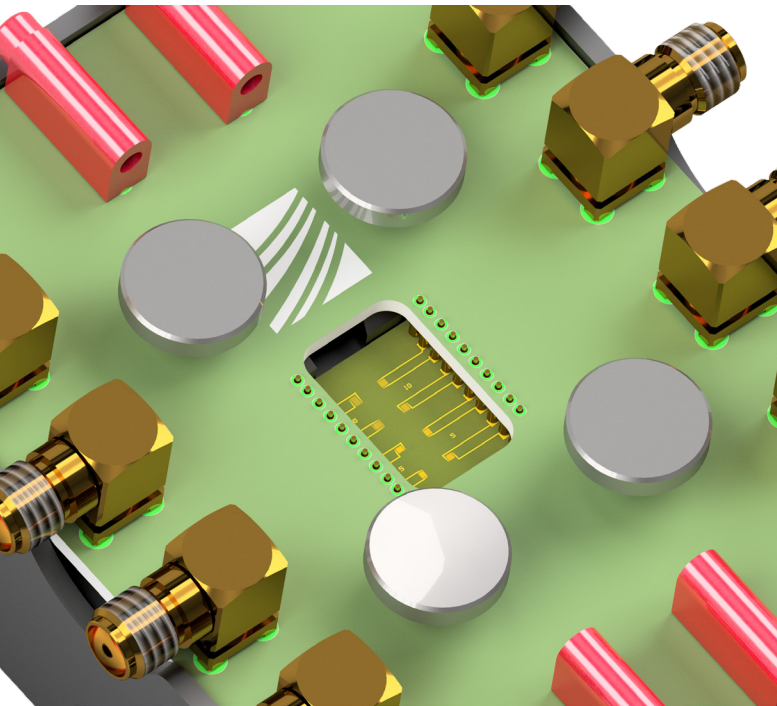


◀ **Figure 2:** Chip AX1580

Part-ID 2030: Diced wafer on foil, 112 Chips
Part-ID 2036: Wafflepack 4x4, 16 Chips



▲ **Figure 3:** Schematic representation of the chip cross-section



Other metals, dielectrics, or electrode geometries are available upon customer request. Measuring adapter for easy contacting of 8 source/drain pairs and a common gate electrode
compatible with AX1580 design:

- Silicon based chips 15x15 mm²
- Gold/ITO interdigital structures for Source/Drain
- Common Gate (n-doped Silicon)
- SiO₂ dielectric 90 nm and 230 nm
- Channel lengths 2,5; 5; 10 and 20 μm
- Channel widths 10 μm
- Voltage range S/D vs. Gate: depends on G_{ox} type and thickness
- Customized designs possible!

Contact

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