Annex A

Item: OFET/LOFET – Substrates, Structures and Measuring Adapter
Short title: OFET/LOFET 2025
Recipient:

Fraunhofer IPMS offers various OFET/LOFET substrates and structures intended for coating with organic semiconductors. All deliveries are A-Samples according to the Fraunhofer IPMS Sample Definition (Annex C).

1. Overview

OFET design	Application	PartID	Chapter
bare OFET without metallization	• Processing and deposition of electrode material by the customer • e.g. top gate OFET or special electrode design	2367 2773	2.1.
OFET Gen4, 230 nm SiO2	• characterization of organic semiconductors with low/medium charge carrier mobility, e.g. pentacene • mainly used for measurement of conductivity	1301 1897	2.2.1.
OFET Gen4, 90 nm SiO2	• characterization of organic semiconductors with low/medium charge carrier mobility, e.g. pentacene • mainly used for measurement of conductivity and OFET transistor behavior with gate contact	2017 2028	2.2.2.
OFET Gen5, 230 nm SiO2	• characterization of organic semiconductors with high charge carrier mobility ($\gtrapprox 10^{-2}$ cm²/Vs) • mainly used for measurement of conductivity	175	2.2.3.
OFET AX1579	• increased transistor length to reduce surface effects • evaluation of surface treatment in channels between electrodes	2472 2035	2.2.4.
OFET AX1580	• same transistor design than OFET Gen4 • Position of Bondpads near the edges of the OFET chip → easy wire bonding of chip e.g. for sensors application → glass encapsulation of active area	2030 2036	2.2.5.
OFET AX1581	• same transistor design than OFET Gen4 • Chip-integrated fast heating of the semiconductor	2031 2037	2.2.6.
LOFET	• demonstration of semiconductor performance	267	2.3.
OFET Prober	• easy and fast interface from your OFET to your measurement systems	990	2.4.

Annex A

2. Specifications

2.1. OFET-Substrates with SiO2 gate-insulator

2.1.1. Gate Oxide 230 nm (Item Number: 2367)

Substrate:	200 mm wafer acc. to semi-standard (used for bottom-gate)
Layer structure:	
Gate:	n-doped silicon (doping at wafer surface: n~3e17 cm^{-3})
Gate oxide:	**230** nm ± 10 nm SiO_2 (thermal oxidation)
Drain/source:	none
Protection:	resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
Layout:	bare oxide but cut
Chip size:	15 x 15 mm²
No. of chips:	112 per wafer
Delivery:	diced wafer on foil, air tight packaging, shipment by Fraunhofer IPMS

2.1.2. Gate Oxide 90 nm (Item Number: 2773)

Substrate:	200 mm wafer acc. to semi-standard (used for bottom-gate)
Layer structure:	
Gate:	n-doped silicon (doping at wafer surface: n~3e17 cm^{-3})
Gate oxide:	**90** nm ± 10 nm SiO_2 (thermal oxidation)
Drain/source:	none
Protection:	resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
Layout:	bare oxide but cut
Chip size:	15 x 15 mm²
No. of chips:	112 per wafer
Delivery:	diced wafer on foil, air tight packaging, shipment by Fraunhofer IPMS

2.2. OFET-Structures on silicon with Au source/drain and SiO2 gate-insulator

2.2.1. Generation 4 - 230 nm SiO_2

Substrate: 200 mm wafer acc. to semi-standard (used for bottom-gate)
Layer structure:
- Gate: n-doped silicon (doping at wafer surface: n~3e17 cm^{-3})
- Gate oxide: **230 nm** ± 10 nm SiO_2 (thermal oxidation)
- Drain/source: 35 nm Au with 10 nm high work function adhesion layer (ITO, structured by lift-off technique)
- Protection: resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
- Layout: see figures 1 and 2
- Chip size: 15 x 15 mm²
- No. of transistors: 16 per chip
  - 4 x transistors L=2.5 µm, W=10 mm
  - 4 x transistors L= 5 µm, W=10 mm
  - 4 x transistors L= 10 µm, W=10 mm
  - 4 x transistors L= 20 µm, W=10 mm
- Contact pads: 0.5 x 0.5 mm²
- Compatibility: fully compatible with OFET Prober

Package	Description	Number of Chips per package
Item Number: 1301	diced wafer on foil, air tight packaging	112
Item Number: 1897	Wafflepack 4x4, air tight packaging	16

2.2.2.Generation 4 - 90 nm SiO_2

Substrate: 200 mm wafer acc. to semi-standard (used for bottom-gate)
Layer structure:
- Gate: n-doped silicon (doping at wafer surface: n~3e17 cm^{-3})
- Gate oxide: **90 nm** ± 10 nm SiO_2 (thermal oxidation)
- Drain/source: 35 nm Au with 10 nm high work function adhesion layer (ITO, structured by lift-off technique)
- Protection: resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
- Layout: see figures 1 and 2
- Chip size: 15 x 15 mm²
- No. of transistors: 16 per chip
  - 4 x transistors L=2.5 µm, W=10 mm
  - 4 x transistors L= 5 µm, W=10 mm
  - 4 x transistors L= 10 µm, W=10 mm
  - 4 x transistors L= 20 µm, W=10 mm
- Contact pads: 0.5 x 0.5 mm²
- Compatibility: fully compatible with OFET Prober

Package	Description	Number of Chips per package
Item Number: 2017	diced wafer on foil, air tight packaging	112
Item Number: 2028	Wafflepack 4x4, air tight packaging	16

2.2.3. Generation 5 (Item Number: 175)

Substrate: 150 mm wafer acc. to semi-standard (used for bottom-gate)
Layer structure:
- Gate: n-doped silicon (doping at wafer surface: n~3e17 cm^{-3})
- Gate oxide: **230 nm** ± 10 nm SiO_2 (thermal oxidation)
- Drain/source: 30 nm Au with 10 nm high work function adhesion layer (ITO, structured by lift-off technique)
- Protection: resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
- Layout: see figures 3 and 4
- Chip size: 15 x 15 mm²
- No. of chips: 60 per wafer
- No. of transistors: 16 per chip
  - 4 x transistors L=2.5 µm, W=2 mm
  - 4 x transistors L= 5 µm, W=2 mm
  - 4 x transistors L= 10 µm, W=2 mm
  - 4 x transistors L= 20 µm, W=2 mm
- Contact pads: 0.5 x 0.5 mm²
- Compatibility: fully compatible with OFET Prober
- Delivery: diced wafer on foil, air tight packaging

2.2.4. Generation AX1579 (10-20-40-80)

Substrate: 200 mm wafer acc. to semi-standard (used for bottom-gate)
Layer structure:
- Gate: n-doped silicon (doping at wafer surface: n~3e17 cm^{-3})
- Gate oxide: **230 nm** ± 10 nm SiO_2 (thermal oxidation)
- Drain/source: 35 nm Au with 10 nm high work function adhesion layer (ITO, structured by lift-off technique)
- Protection: resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
- Layout: see figures 5 and 6
- Chip size: 15 x 15 mm²
- No. of transistors: 16 per chip
  - 4 x transistors L=10 µm, W=2 mm
  - 4 x transistors L=20 µm, W=2 mm
  - 4 x transistors L=40 µm, W=2 mm
  - 4 x transistors L=80 µm, W=2 mm
- Contact pads: 0.5 x 0.5 mm²
- Compatibility: fully compatible with OFET Prober

Package	Description	Number of Chips per package
Item Number: 2472	diced wafer on foil, air tight packaging	112
Item Number: 2035	Wafflepack 4x4, air tight packaging	16

2.2.5. Generation AX1580 (Bondpads)

Substrate: 200 mm wafer acc. to semi-standard (used for bottom-gate)
Layer structure:
- Gate: n-doped silicon (doping at wafer surface: n~3e17 cm^{-3})
- Gate oxide: **230 nm** ± 10 nm SiO_2 (thermal oxidation)
- Drain/source: 35 nm Au with 10 nm high work function adhesion layer (ITO, structured by lift-off technique)
- Protection: resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
  - Layout: see figures 7 and 8
- Chip size: 15 x 15 mm²
- No. of transistors: 8 per chip
  - 2 x transistors L=2.5 µm, W=10 mm
  - 2 x transistors L= 5 µm, W=10 mm
  - 2 x transistors L= 10 µm, W=10 mm
  - 2 x transistors L= 20 µm, W=10 mm
- Contact pads: 0.5 x 0.5 mm²
- Compatibility: NOT compatible with OFET Prober

Package	Description	Number of Chips per package
Item Number: 2030	diced wafer on foil, air tight packaging	112
Item Number: 2036	Wafflepack 4x4, air tight packaging	16

2.2.6.Generation AX1581 (Heater)

Substrate: 150 mm wafer acc. to semi-standard (used for bottom-gate)
Layer structure:
- Gate: n-doped silicon (doping at wafer surface: n~3e17 cm^{-3})
- Gate oxide: **230 nm** ± 10 nm SiO_2 (thermal oxidation)
- Drain/source: 100 nm Au with 10 nm high work function adhesion layer (ITO, structured by lift-off technique)
- Protection: resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
  - Layout: see figures 9 and 10
- Chip size: 15 x 15 mm²
- No. of transistors: 16 per chip
  - 4 x transistors L=2.5 µm, W=10 mm
  - 4 x transistors L= 5 µm, W=10 mm
  - 4 x transistors L= 10 µm, W=10 mm
  - 4 x transistors L= 20 µm, W=10 mm
  - inclusive heater
- Contact pads: 0.5 x 0.5 mm²
- Compatibility: measurement works with OFET Prober

Package	Description	Number of Chips per package
Item Number: 2031	diced wafer on foil, air tight packaging	60
Item Number: 2037	Wafflepack 4x4, air tight packaging	16

2.3. LOFET 3 substrates (Item Number: 267)

Wafer:	150 mm according SEMI standard
Structure classes:	transistors, inverters, and ring oscillators, additional technology test structures
Layout:	see figure 11
Die size:	15 x 15 mm²
Number of dies:	56
Number of pads:	39 + 2
Pad size:	1200 x 800 µm²
Gate oxide:	200 nm ± 10 nm
Structured layers:	3 (gate, contacts, source/drain)
Source/drain layer:	Ti/TiN, Rs about 10 Ω/sq.
Contacts:	standard 20 x 20 µm², R about 20 Ω
Top layer:	70 nm Au with 10 nm high work adhesion layer (ITO, structured by lift-off technique), Rs about 0.65 Ω/sq. / 0.45 Ω/sq.
Resist protection layer:	resist AR PC 5000/3.1 (soluble in AZ-Thinner or acetone)
Documentation:	included in shipment
Shadow mask:	possible, but not required
Probe card:	possible, but not required
Compatibility:	NOT compatible with OFET Prober
Delivery:	diced wafer on foil, air tight packaging

2.4. OFET Measuring Adapter for OFET-Structures (short OFET prober, Item Number: 990)

In order to simply and quickly measure OFET components with a given substrate size, pad grid and pad arrangement in large batches, Fraunhofer IPMS has developed a miniprober. It has two electric connections on the front (source and drain) and one connection on the back (gate) and does not require samplers, manipulator pins or microscopes. See figures 12 and 13.

Size:	120 x 110 x 35 mm³
Probe card size:	40 x 76 x 17 mm³
Material:	aluminium C250, FR4; plastics
Probe card type:	"OFET" 2 pieces miniature spring contact 6A
Weight:	280 g
Connection:	BNC panel jack
Compatibility:	with parts 175,1301,1897, 2017, 2028, 2029, 2035, 2031, 2037, 2472
Delivery:	in plastic case including manual

3. Figures

3.1. OFET-Structures on silicon with Au source/drain and SiO2 gate-insulator Generation 4

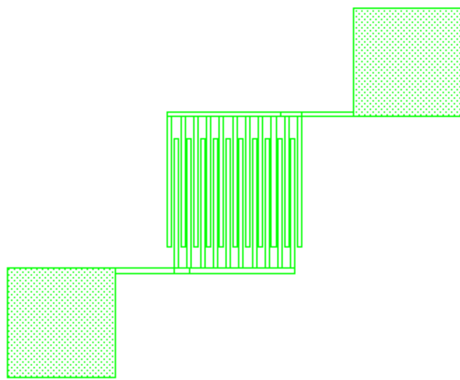

Figure 1: Layout of a single transistor (Gen. 4)

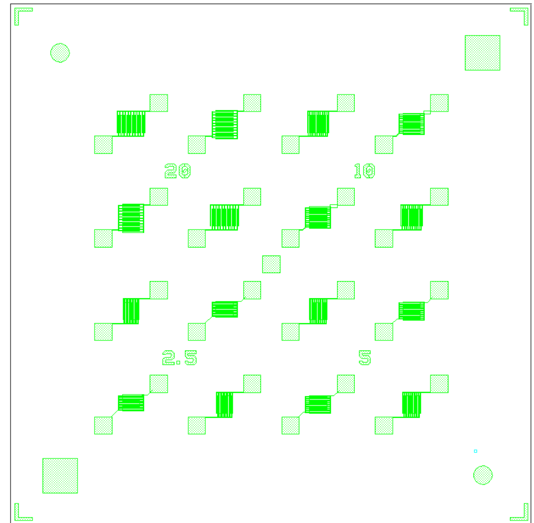

Figure 2: Layout of chip 15 x 15 mm² (Gen. 4)

3.2. OFET-Structures on silicon with Au source/drain and SiO2 gate-insulator Generation 5

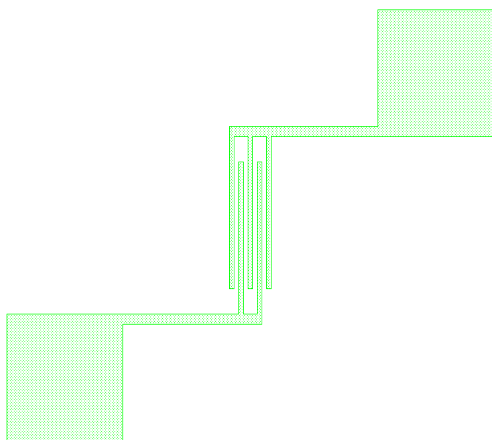

Figure 3: Layout of a single transistor (Gen. 5)

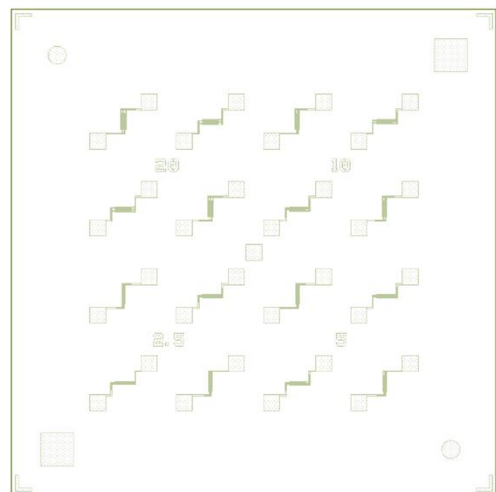

Figure 4: Layout of chip 15 x 15 mm² (Gen. 5)

3.3. Generation AX1579 (10-20-40-80)

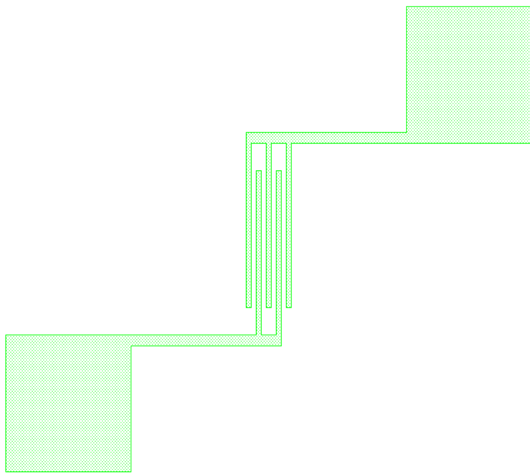

Figure 5: Layout of a single transistor (AX1579)

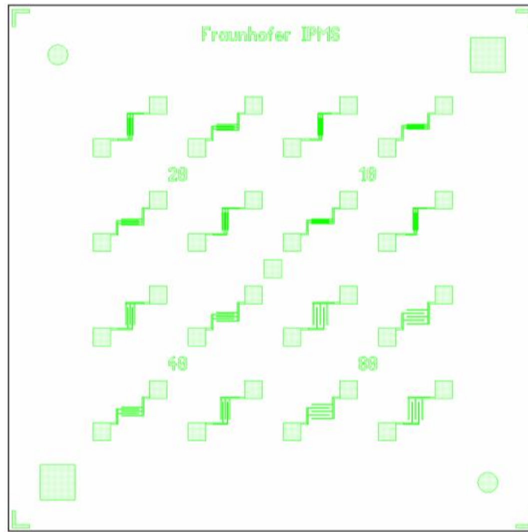

Figure 6: Layout of chip 15 x 15 mm² (AX1579)

3.4. Generation AX1580 (Bondpads)

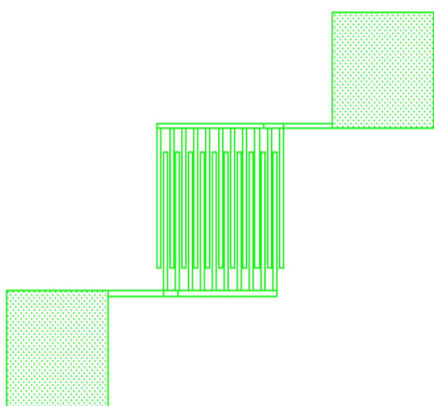

Figure 7: Layout of a single transistor (AX1580)

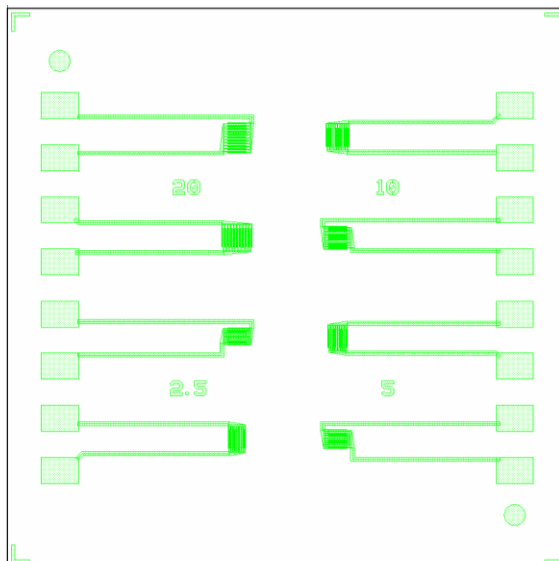

Figure 8: Layout of chip 15 x 15 mm² (AX1580)

3.5. Generation AX1581 (Heater)

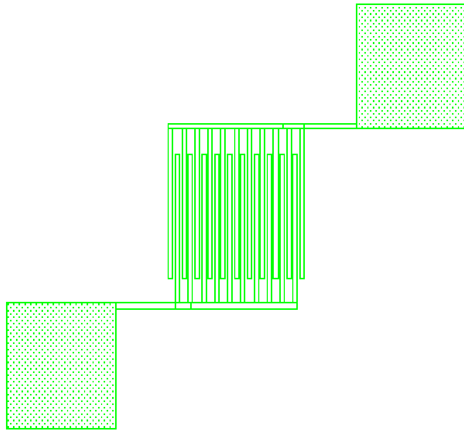

Figure 9: Layout of a single transistor (AX1581)

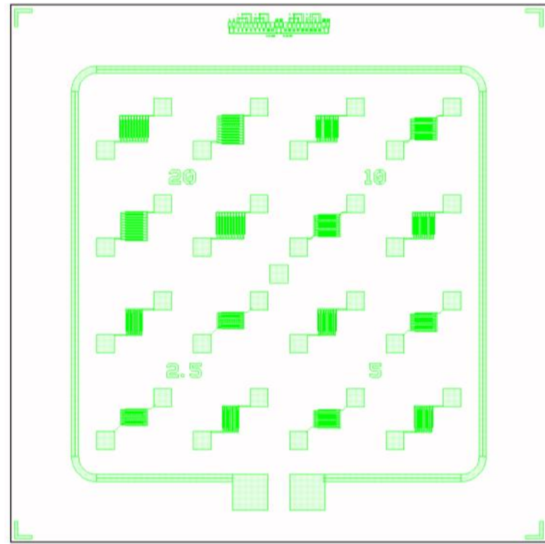

Figure 10: Layout of chip 15 x 15 mm² (AX1581)

3.6. LOFET 3 substrates

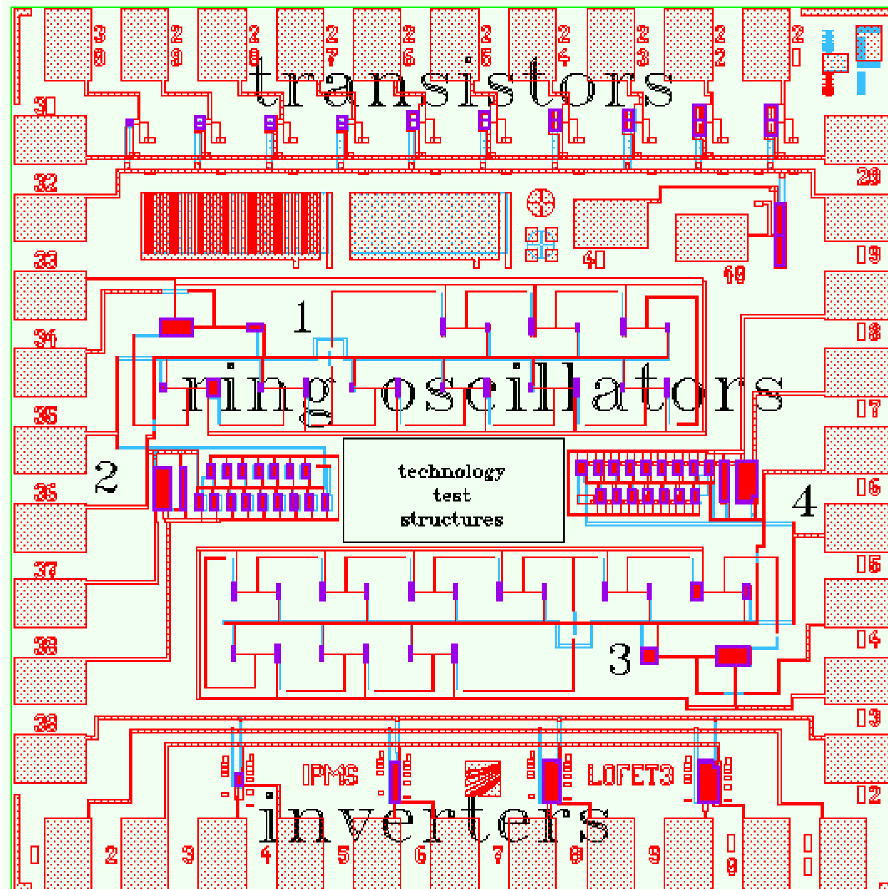

Figure 11: Layout “LOFET 3”

3.7. OFET Measuring Adapter

Figure 12: OFET Measuring Adapter

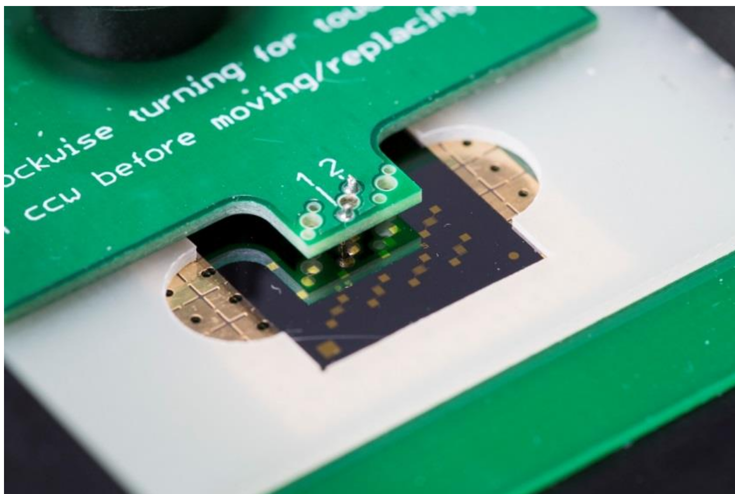

Figure 13: OFET Chip attached to OFET Measuring Adapter