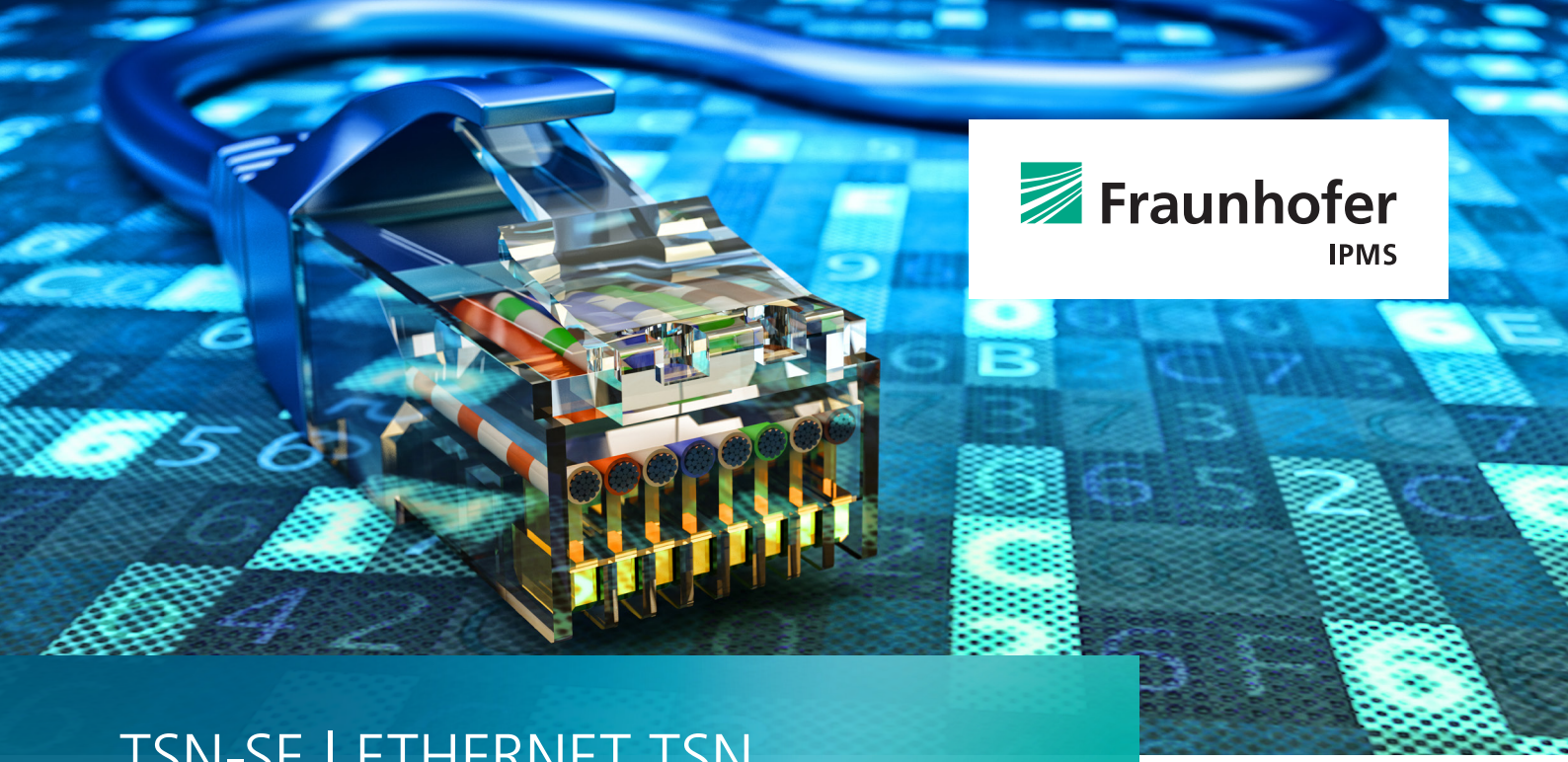


Fraunhofer IPMS

TSN-SE | ETHERNET TSN SWITCHED ENDPOINT CORE

Time-Sensitive Networking (TSN) is a set of sub-standards that enhance the existing Ethernet specification towards time synchronization and deterministic communication in switched networks according to existing IEEE 802.1 and 802.3 standards. The goal is it to make Ethernet more suitable for the advancing needs of industrial and automotive applications. The TSN Ethernet IP core TSN-SE provides TSN switched endpoint functionality and eases the integration of devices into networks complying with the TSN standards. Two external 10/100/1000 Mbits/s ports are available beside an internal CPU port. The design implements a 1 GbE switching bar with cut-through capability. It provides time-sensitive networking for full-duplex point-to-point Ethernet communication enabling daisy chaining, devices, ring architectures or physical redundant communication. The IP core consists of two instances of the TSN-EP IP and a switching bar as well as additional routing logic optimized for low latency communication.

Several hundreds of customers worldwide have relied on the quality of Fraunhofer IPMS IP-Core solutions for FPGA and ASIC designs and the comprehensive technical support for over 20 years.

Applications

The TSN-SE IP Core is suitable for the implementation of talkers and listeners within TSN Ethernet networks. The TSN-SE IP can be utilized for embedding real-time TSN applications into regular Ethernet networks. It is suitable for daisy-chained networks such as rings.

It is targeting for applications in industrial automation, robotics, automotive, aerospace and more.

Verification

Interoperability of sub-modules is constantly tested within TSN plug-fests by LNI4.0 and Industrial Internet Consortium (IIC).

industrial internet CONSORTIUM

LNI4.0 LABS NETWORK INDUSTRIE 4.0

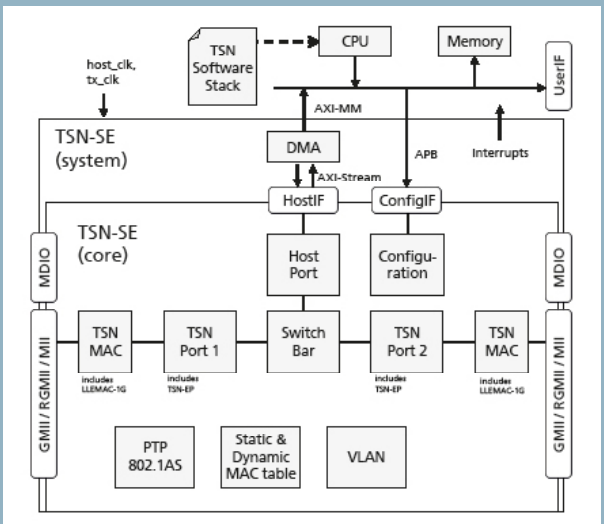
Contact

Monika Beck
+49 351 88 23 - 274
monika.beck@ipms.fraunhofer.de

Dr. Frank Deicke
+49 351 88 23 - 385
frank.deicke@ipms.fraunhofer.de

Fraunhofer Institute for
Photonic Microsystems IPMS
Maria-Reiche-Str. 2
01109 Dresden
Germany

www.ipms.fraunhofer.de



Schematic diagram of the TSN-SE IP Core.

TSN Features

- Time synchronisation (IEEE 802.1 AS-2020)
- Traffic-Shaping (IEEE 802.1 Qav and Qbv)
- Frame Preemption (IEEE 802.3br and IEEE 802.1Qbu)
- Frame Replication and Elimination (IEEE 802.1CB)
- SRP Enhancements (IEEE 802.1Qcc)
- Stream Filtering and Policing (IEEE 802.1Qci)
- Ethernet MAC communication (IEEE 802.3)
- IPMS AXI4-DMA core optional

Easy Integration

- Platform independent implementation into any FPGA or foundry technology
- TSN-SE IP core can be attached to custom SoC, or a complete TSN-SE can be provided
- Intel & Xilinx based evaluation platforms
- Set of demo projects for Xilinx and Altera
- Configurable feature set
- Responsive support
- TSN Evaluation Kit available

IEEE 802.1Q Switch Features

- Layer 2 switch cut-through architecture
- 2 Gigabit TSN ports and 1 host port
- Supports up to 1024 dynamic and 1024 static MAC table entries
- Supports IEEE 802.1Q VLAN-tags with up to 1024 entries
- Ports run full-duplex at 10/100/1000 Ethernet
- PHY configuration via MDIO

Deliverables

- Verilog RTL source code or targeted FPGA netlist
- Testbenches
- Sample simulation and synthesis scripts
- Comprehensive documentation
- TSN FreeRTOS Unified Framework, CLI example, PTP-AS2020
- FreeRTOS example projects
- Linux driver reference design

Designed for Usage with Ethernet MACs

- ALTERA/Intel Triple Speed Ethernet MAC
- XILINX Tri-Mode Ethernet MAC
- IPMS Triple Speed Low-Latency Ethernet MAC
- Triple speed: 10 / 100 / 1000 Mbit/s Ethernet
- 2.5/5/10+ Gbps on request
- PHY Interfaces to MII, GMII and RGMIII
- Ingress latency: 6 Rx clock cycles
- Egress latency: 10 Tx clock cycles

Data Interfaces

- Advanced Peripheral Bus (APB) for memory mapped register access
- 2 – 8 AXI-Streams for TX data (configurable byte width)
- 1 AXI-Stream for RX data (configurable byte width)
- Avalon interfaces available
- More interfaces upon request

TSN Evaluation Xilinx ZCU102 or Intel Netleap (Cyclone V SoC); implemented IPMS TSN-IP core for switched endpoint applications (TSN-SE).