Fraunhofer IPMS

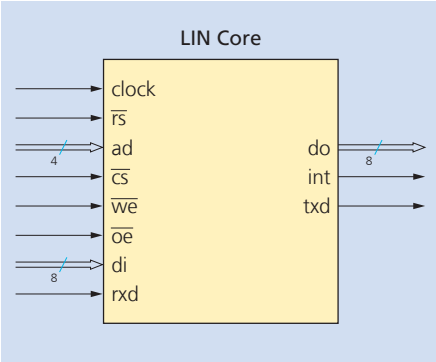
LIN-CTRL

LIN Controller Core

LIN (Local Interconnect Network) is a serial communication protocol mainly used in low cost automotive networks. It enables cost-efficient bus communication within applications like Automotive networks, but also industrial.

It can be implemented as a master or slave and operate on a LIN 1.3, 2.0, 2.1 or 2.2 LIN network. A single master/multiple slave concept is used for transfer of messages between nodes of the LIN network. The transfer can be controlled via a microcontroller interface and a LIN transceiver is needed for the connection to the LIN bus.

Also a safety-enhanced package is available. It implements ECC for SRAMs protection and uses spatial redundancy for protecting the inner logic of the core. The Safety-Enhanced versions are certified as ISO-26262 ASIL-D ready.



LIN core pinout.

Contact

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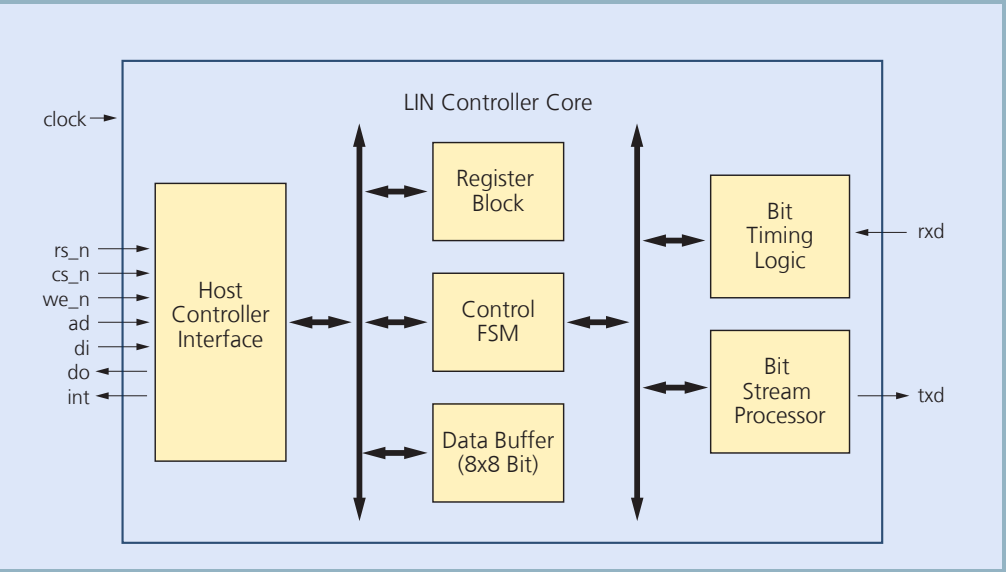

LIN system with one master and two slaves.

Features

- Support of LIN specification 2.2A, backwards compatible to LIN 1.3
- Programmable data rate between 1 Kbit/s and 20 Kbit/s
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface
- Configurable for support of master or slave functionality
- Slave can be implemented with or without clock synchronization
- Fully synchronous VHDL or Verilog design, completely synthesizable
- ISO 26262 ASIL D ready

Verification

It has been embedded into several customer products, and is proven in both ASIC and FPGA technologies.

Safety Enhanced Package

- SAM and FDMEA certified ISO-26262 ASIL D ready
- ISO-26262 documentation package

Easy System Integration

- Platform independent implementation into any FPGA or foundry technology
- Silicon proven
- Responsive implementation support

Deliverables

- VHDL or Verilog RTL source code
- Post-synthesis netlist for FPGA
- Testbenches (behavioral, post-synthesis verification)
- Simulation and synthesis scripts
- Safety enhanced version available
- ISO26262 ASIL-D ready safety package
- Documentation