PRESS RELEASE

RISC-V development at Fraunhofer IPMS

Flexibility, durability and trust - RISC-V conquers the processor market

The accessibility of RISC-V has started a revolution and, thanks to its open architecture, allows developers to design processors tailored to specific requirements. The Fraunhofer IPMS also offers a processor IP based on the RISC-V instruction set architecture. The institute has extensive RISC-V expertise, which is used in research projects and is actively developed.

The open-source instruction set architecture (ISA) called "Reduced Instruction Set Computer V" (RISC-V) was designed with the aim of emphasizing energy efficiency in addition to computing power for new designs. This enables small, energy-efficient and at the same time high-performance processors. Because the ISA is freely available, companies can design, customize, and implement RISC-V processors.
The Fraunhofer IPMS has also developed a processor IP based on the open RISC-V ISA. The EMSA5 is a 32-bit processor with a five-stage pipeline that is used in embedded systems as well as in functional safety applications such as in the automotive sector. For the latter, the IP core has an ASIL D ready certification according to ISO 26262.
The know-how of the Fraunhofer IPMS development team about the RISC-V ecosystem is also used and further developed in research projects.

Fraunhofer IPMS contributes RISC-V expertise to research activities

Research project Tristan

The overarching goal of the BMBF-funded project TRISTAN is to expand and industrialize the European RISC-V ecosystem. For this purpose, the ecosystem will be extended with essential components in industrial-quality, which can be used for SoC designs in various application areas (e.g. automotive, industrial, etc.). The approach includes both electronic design automation (EDA) tools and the entire software stack. This will provide an independent and open alternative to commercial - mostly non-European - solutions and strengthen Europe's technological sovereignty.

In the project the Fraunhofer IPMS together with other partners will develop an open source trace module for embedded RISC-V processors based on appropriate specifications. This trace IP will be integrated into a demonstrator together with the

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RISC-V processor EMSA5 and a TSN-capable Ethernet endpoint IP in order to demonstrate trouble-free tracing while the user application on the processor simultaneously uses the interface.

Research project ImaB Edge

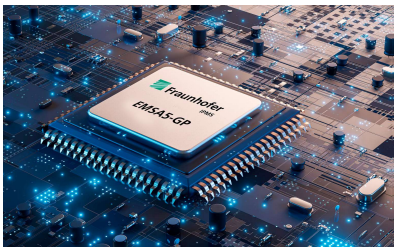
As part of the OCTOPUS funding program, the joint project ImaB-Edge is developing a system of distributed sensor electronics for permanent monitoring of the condition of the structural fabric of infrastructure buildings in order to ensure energy-efficient and predictive maintenance. The project thus contributes to the safety of infrastructure and its cost-saving maintenance.

The main task of the Fraunhofer IPMS is the design of an energy-efficient, flexibly scalable and yet very high-performance computing cluster consisting of several RISC-V processors. The EDGE gateway serves as a self-sufficient data acquisition module for the permanently installed sensor EDGE modules and as a central interface module for the operator. Using artificial intelligence, it is designed to provide up-to-date a priori knowledge. The findings are also combined with historical data. In addition, the EDGE gateway will implement the integration of expert knowledge into the sensor system.

About Fraunhofer IPMS

Fraunhofer Institute for Photonic Microsystems IPMS has more than 20 years of experience in design and licensing of IP cores with several hundred users worldwide in various automotive, aerospace and industrial applications with a special focus on functional safety. The institute offers platform-independent IP core modules that can be implemented in all FPGA types and ASIC technologies. The IP cores enable designers to quickly embed complete functional areas in standard products such as SoCs, microcontrollers, FPGAs and ASICs, thus significantly reducing development time and costs. In addition to the standard IP cores, Fraunhofer IPMS also offers customized design adjustments or develops systems based on specific customer requirements.

Images



RISC-V processor core EMSA5-FS
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