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1 *Reference of an example micro system.*

2 *Selected defective chips of an example micro system.*

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AUTOMATED OPTICAL INSPECTION (AOI) OF MICRO SYSTEM DIES

Motivation

The Fraunhofer Institute for Photonic Microsystems IPMS in Dresden is developing and fabricating micro system chips based on silicon wafers and technologies similar to semiconductor electronics. These products have often optical or sensory active surface regions or tiny mechanical structures that have to be proved for quality, but cannot be tested electrically. Therefore, optical inspection is necessary to complement electrical testing for full quality assurance. Fig. 1 illustrates an exemplary micro system and possible defects that are optically visible. Small quantities of such chips can be inspected visually through a microscope. However, this method is limited in through-put, and the results depend significantly on the skills and mental vigor of the persons actually performing the tests.

Therefore, in order to test large quantities of micro system chips highly reproducible, Fraunhofer IPMS has developed a wafer probing setup for automated optical testing. Since wafer probers are usually equipped with controllable precision cross tables and adjustment microscopes, they are ideally suited to attach optical testing features based on digital imaging.

Hardware Setup

The probing equipment consists of a wafer prober of PA-200 SUSS MicroTec, a Mitutoyo FS70Z Microscope with M Plan Apo 5x long working distance objective, a high resolution IEEE1394 digital camera A102fc from BASLER Vision Technologies, and a standard computer with a MATROX framegrabber. The cross table carries a
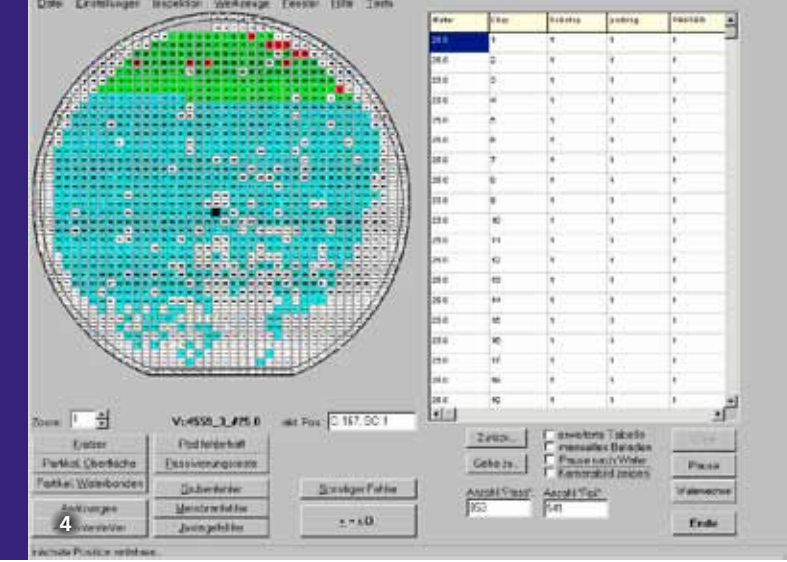
wafer fixing stage that fits to several types of wafers, the wafer dismount and mount step has still to be performed manually, but can be potentially automated, too. A photograph of the prober setup is shown in Fig. 2.

Software

The optical test software called VITool (Visual Inspection Tool) controls the cross table movement across the wafer according to the chip positions, the image capturing and its processing by calling a chip-specific Dynamic Link Library (DLL). The DLL executes the analysis algorithm specific for the chip and accesses the MATROX MIL Imaging Library. The interface between both layers is defined in such a way that all testing

options and parameters are adjustable interactively or per configuration file without any change of the program code. Finally, the binary result of the optical inspection (pass or fail) is stored in the wafer map. Each chip must pass through both electrical and optical testing in order to be used and processed further. The graphical user interface of the VITool (Fig. 3) visualizes the testing progress and yield trend while processing a wafer.

Some chips have very fine structures to be investigated, which cannot be resolved in an image of the entire chip. In that case the chip has to be partitioned and captured step by step (e.g. half or quarter chip), and the image parts are accurately stitched together before analysis. Fig. 4 illustrates such a fine-grained example structure.

Fields of Application

The test equipment characterized above is used for quality control of a couple of products that Fraunhofer IPMS supplies for its key accounts. These are:

- Micro Electro (Opto) Mechanical System (MEMS/MOEMS) devices
- Micro-machined pressure sensors
- Photo detector arrays for optical measurement systems
- Organic light emitting diodes (OLED), also for measuring the homogeneity of the luminous density
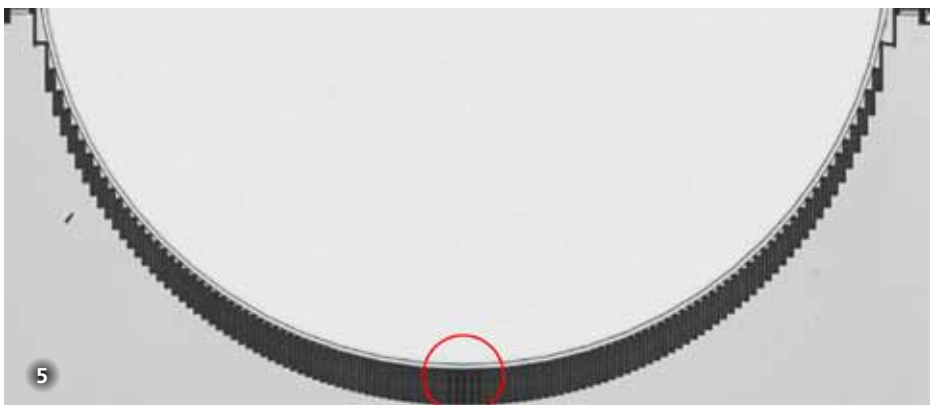
3 *Photograph of the automated optical inspection setup.*
4 *VITool snapshot of a test run in progress: green means pass-, red means fail-chip, blues ones are not tested yet.*
5 *Fine-grained comb structure of a MEMS that requires image partitioning.*