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FRAUNHOFER INSTITUTE FOR PHOTONIC MICROSYSTEMS IPMS

MEMS REPORT

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CONTENTS

OFET Substrates: End-of-line Standard Substrates for the Characterization of Organic Semiconductor Materials
Vacuum Encapsulation of Micro Mirrors at Wafer Level
In Situ Topographic Measurement of Micro Mirror Arrays
Smart-Tank Makes Monitoring and Optimization of Biogas Processes Possible

◄ Cover picture: Fraunhofer IPMS clean room for microsystems



Prof. Dr. Hubert Lakner
Director of Institute

Dear Customers, Partners and Friends
of Fraunhofer IPMS,

Our MEMS Report is now moving into its second year. At first glance, the focus of this first edition is a rather surprising topic: test substrates for organic field effect transistors (OFETs). However, thanks to the possibilities our MEMS clean room offers, it has been possible for us to provide customers with standardized single transistor structures for many years. These can be used by chemists, process developers and circuit designers for simple and reliable electronic tests to characterize active organic semiconductor materials. The strong increase in the demand for our OFET/LOFET services in the past year has impressed upon us how interesting our technologies are for customers.

Intensive information sharing with you is very important to us in order to identify further attractive fields of research. It would make me very pleased if this MEMS Report were to play a part in initiating discussions with you. The opportunity for one-on-one discussions with our employees will certainly present itself at our trade shows over the next few weeks, to which we warmly welcome you.

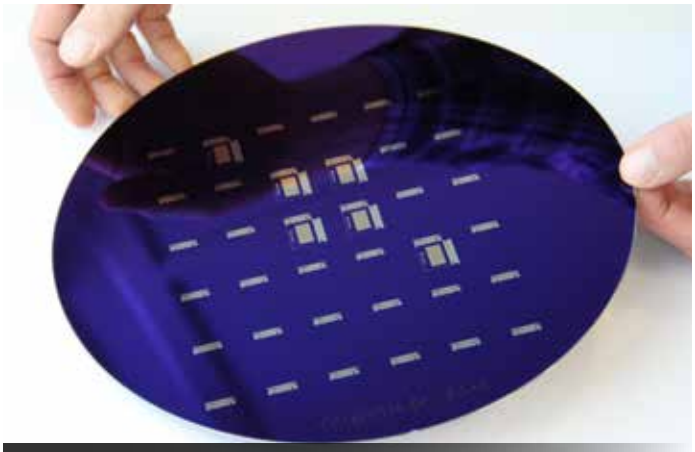


Prof. Dr. Hubert Lakner

QUICK NOTES

Fraunhofer CNT Becomes a Department of Fraunhofer IPMS

The Fraunhofer-Gesellschaft Senate has decided to cease operation of the Fraunhofer Center Nanoelectronic Technologies CNT as an independent entity, effective January 1, 2013. Prof. Hubert Lakner, Director of the Fraunhofer IPMS and Chairman of the Fraunhofer Group for Microelectronics, was entrusted with the re-orientation of the Fraunhofer CNT. At the same time, he also took over its management. The Fraunhofer CNT will retain its location in close vicinity of Infineon, will however now be set up, in terms of organization, as a department of the Fraunhofer IPMS and strategically re-oriented.

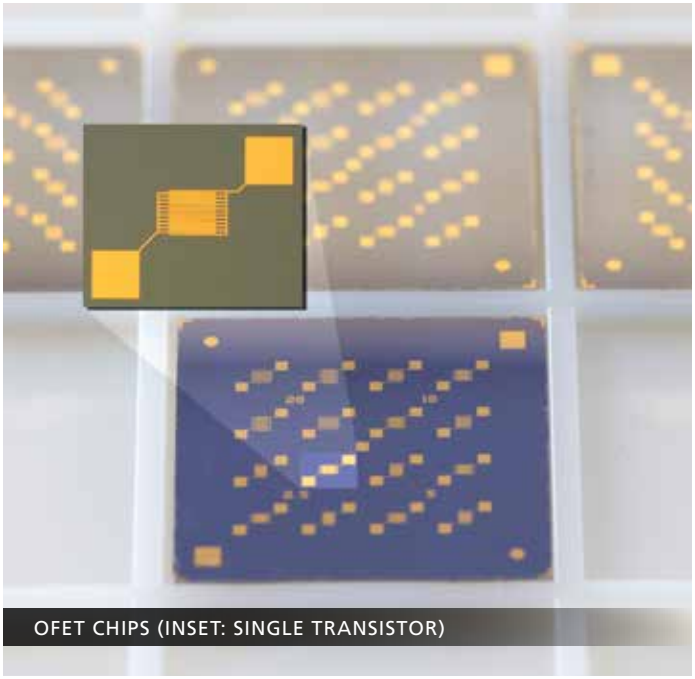


THE NEW DEPARTMENT WORKS WITH 300 MM WAFERS

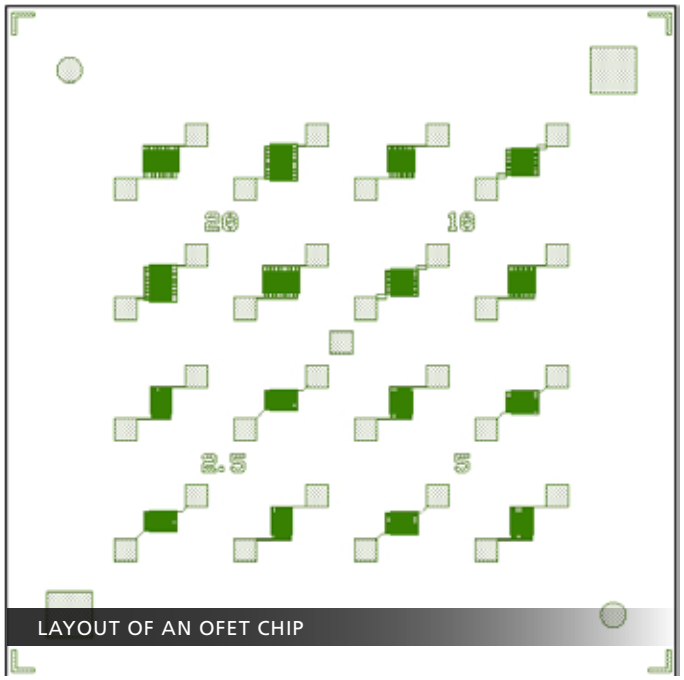
Fraunhofer IPMS' Invitation to Training Course "MEMS Scanning Mirrors"

On June 17, 2013, Fraunhofer IPMS is offering a training course on technologies and applications for MEMS scanning mirrors. The seminar will introduce the basics of MEMS scanner technology using the Fraunhofer IPMS scanners and will also present the potential of the technology in particular. Along with teaching the basics, special scanners for sample applications will be emphasized. After the seminar, the participants will be able to specify MEMS scanners for their own applications and also estimate the feasibility of MEMS scanner-based solutions and products. The seminar is directed especially at engineers and product developers. Further information and registration forms are available for download on the Fraunhofer IPMS website. Registration is still possible and ends on May 20, 2013.

OFET SUBSTRATES: END-OF-LINE STANDARD SUBSTRATES FOR THE CHARACTERIZATION OF ORGANIC SEMICONDUCTOR MATERIALS



OFET CHIPS (INSET: SINGLE TRANSISTOR)



LAYOUT OF AN OFET CHIP

Over the last few years organic electronics have become a keyword for new types of applications based on organic semiconductors and other materials that can easily be processed. Typical for this new class of materials are low temperature processes and large area deposition and structurization with various coating and printing processes. The active semiconductor materials determine the performance of the entire system considerably. That is why a simple and reliable electronic characterization of these semiconductors is not only an essential prerequisite for material development in the labs of organic chemists but also for process developers and circuits designers.

For material analysis in the field of organic semiconductors, the Fraunhofer IPMS provides standardized single transistor structures in bottom gate architecture. These substrates for organic field effect transistors (OFETs) are produced in the clean room on silicon wafers with thermal silicon-dioxide (SiO_2) as full-area dielectrics and gold electrodes in lift-off technology (Figure, upper left).

If a semiconductor layer is deposited on such a substrate, the Si-bulk acts as gate electrode and controls the channel current between the gold electrodes on top. A suitably doped Si-SiO_2 interface in CMOS quality guarantees a reproducible gate contact. Gold electrodes with a patented undercoating suppress the formation of injector barriers between the gold electrodes and the organics in the transistor channel. This guarantees reliable ohmic source/drain contacts in the OFET even for p-type semiconductors.

In the standard layout, each 150 mm wafer yields 960 individual transistors on 60 chips, each sized at 15 × 15 mm². Each chip carries four groups with four identical transistors, with a channel length of 2.5, 5, 10 and 20 µm respectively (Figure above). Identical layouts with graded channel widths as well as a flexible selection of the oxide thickness allow the adjustment to a broad voltage and conductivity range of the test materials. Customer specific layouts with different electrode geometries are possible at any time.

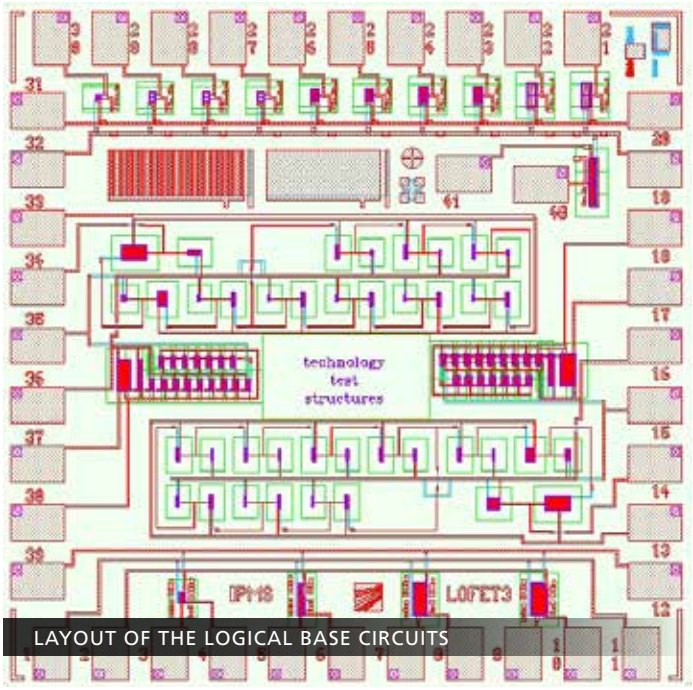
Due to both reliability and reproducible preparation, these substrates are applied for standardized material screening by all key developers of organic semiconductors all over the world.

Logical Base Circuits with OFET (LOFET)

One further step in simplifying materials characterization is the analysis of logical base circuits. Here, up to 36 single transistors are interconnected to inverter and ring oscillators. Monitoring of the active materials then only requires a frequency measurement of the ring oscillators which can be automated easily. The much more complicated measurement and analysis of the individual transistor characteristic is unnecessary. Furthermore, it is not only reliable

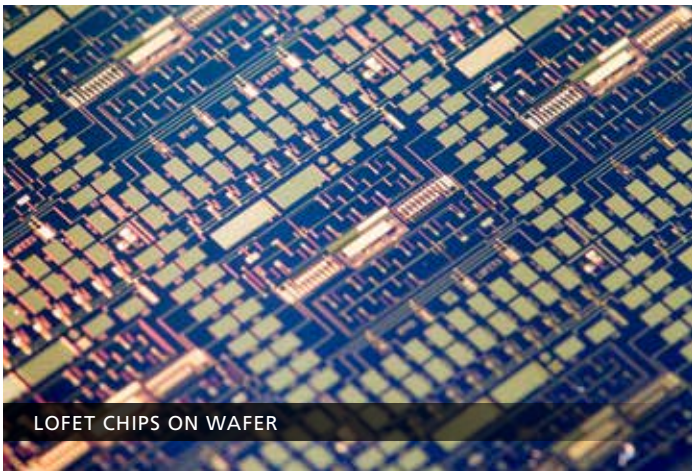
information about logic capability that is acquired. The dynamic characteristics of the inverters are also determined.

The layout shown in the figure below includes an initial block with eleven individual transistors making a complete parameter extraction for circuit simulation possible. A second block contains four inverters which are replicated in the oscillators. These separately accessible inverter levels enable a detailed analysis of the transient behavior in case the amplification of the individual inverter stages is not sufficient for starting the oscillation of the ring oscillators. The third block contains ring oscillators with either seven or 15 stages. Each ring circuit has a three-stage output amplifier which decouples the oscillation inside of the ring from the output terminal and allows a direct frequency measurement without external amplification. Although only two geometric variations for the driver to load ratio are present, an external load control on the gate terminal of the load transistors makes adjustment over a broad semiconductor performance range possible.



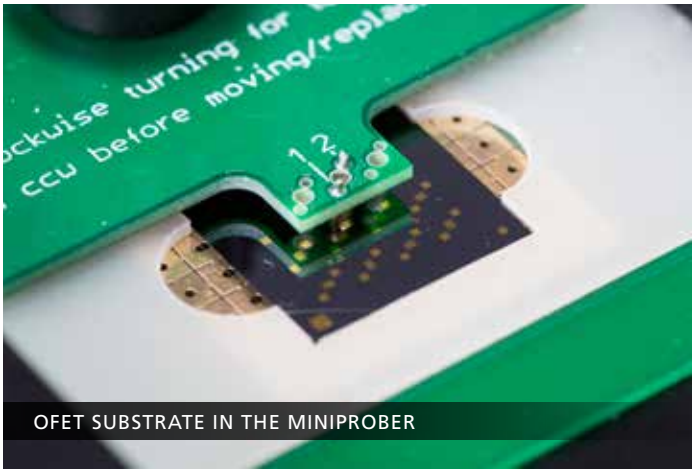
LAYOUT OF THE LOGICAL BASE CIRCUITS

The LOFET substrates are also produced in bottom gate architecture so that functional circuits require the deposition of the semiconductor layer only. In order to realize the wiring of the transistors, a 3-mask-layer process is indispensable. These three layers are a Ti/TiN gate metal, a 200 nm thick SiO_2 dielectric with contact holes, and a gold/ITO source drain metallization known from the OFET substrates. Using a fourth mask layer for structuring the semiconductor enables a separation of all single transistors as well as the transistors within selected inverters and ring oscillators. This may be used for suppressing parasitic cross currents between adjacent transistors of the stages.


LOFET CHIPS ON WAFER

The OFET MINIPROBER

In order to simply and quickly measure OFET components with a given substrate size, pad grid and pad arrangement in large batches, Fraunhofer IPMS has developed a miniprober. It has two electric connections on the front (source and drain) and one connection on the back (gate) and does not require samplers, manipulator pins or microscopes.


OFET SUBSTRATE IN THE MINIPROBER

A reliable interconnection is established on contact pads, which are only 0.5 mm × 0.5 mm in size. Customized versions of the miniprober varying the connection arrangement, the position and number of the pads are possible. This makes the miniprober suitable for other applications in addition to OFETs. The transmission of the signals to the measurement instrument is done with BNC or triax cables.

FIVE QUESTIONS FOR CARSTEN HOHLBEIN

Fraunhofer IPMS: "The development of OFET substrates already has a long tradition at the Fraunhofer IPMS. How did it start?"

Carsten Hohlbein: "Our initial work in the field of OFET substrates for organic semiconductors started with a BMBF supported project in 2004. In cooperation with the Fraunhofer Research Institution COMEDD, formerly part of Fraunhofer IPMS, we worked on the development of end-of-line standard substrates for the characterization of organic semiconductor materials which were later patented. Although they were only used by Fraunhofer COMEDD initially, we identified great potential in these substrates and began to develop them within an EU project from 2007 onward, establishing a professional manufacturing technology. We were able to build up partnerships and acquire our first customers. We quickly received positive feedback. Based on this we developed demonstrators, sent out customer samples and implemented several modifications, e.g. by varying layer thicknesses. Over time, we have become quite flexible and have thus been able to attain subsequent orders from both industrial and research sectors. The flexibility and promptness is closely connected to the fact that we are still running our pilot manufacturing in cooperation with Fraunhofer IZM and Fraunhofer COMEDD."

Fraunhofer IPMS: "What is special about the developed technology?"

Carsten Hohlbein: "Our unique selling point is the application of a patented semi layer of indium-tin-oxide (ITO) in the substrate structures as well as post-processing with gold in the lift-off process. This material combination has excellent electric characteristics and is very stable, both mechanically and chemically. We also use silicon-dioxide in CMOS quality as the dielectric. That is a significant advantage with respect to reliability and reproducibility that enabled the application of these substrates for quality assurance in major chemical corporations."

Fraunhofer IPMS: "Which customers will this particularly appeal to?"

Carsten Hohlbein: "The spectrum of possible customers is very large and ranges from universities, independent research institutions to industrial customers. The OFET substrates we manufacture are used for research purposes in the field of materials testing or for quality control, respectively. They are essential for organic materials development. In addition, they are also applied in the industrial sector, so we are proud to have two market-listed companies both national and international among our customers. To date, our customer base has grown to 80 customers worldwide, including 15 key customers. Our revenue has doubled since we started. For the future we see further potential growth. The next step will be to appeal to an even broader customer base. That is why we also offer, for example, sample chips to interested parties. As a free service we offer sample chips to companies and research institutions within Europe, outside of Europe only the shipping costs will be charged."



Carsten Hohlbein has been team leader of Production Planning and Control since May, 2004 at Fraunhofer IPMS. In this function, he is in charge of all pilot production projects and responsible for the entire OFET/LOFET manufacturing at the Institute.

Fraunhofer IPMS: "What does your spectrum of services encompass?"

Carsten Hohlbein: "At the moment we offer five different standard solutions, but we started with just one solution. Based on these standard components, we have already realized over 25 customer specific modifications. We are able to tailor our samples with respect to chip size, design, and layer thickness of the thermal oxide. I would like to point out our latest development: substrates for logical base circuits for OFET technology. These substrates simplify material control and testing and allow cost-effective automation."

Fraunhofer IPMS: "What are the advantages of the OFET miniprober developed by Fraunhofer IPMS?"

Carsten Hohlbein: "Nowadays OFET substrates are usually tested by manually placing manipulator pins on the contact pads. Risks lie in inappropriate measurements, which might force incorrect results. In order to simplify these measurement procedures, the Fraunhofer IPMS has developed a hand prober. It allows faster and easier measurements by reliable pad contacting. Its suitability for mobile applications and its small size are further advantages of the OFET miniprober."

VACUUM ENCAPSULATION OF MICRO MIRRORS AT WAFER LEVEL

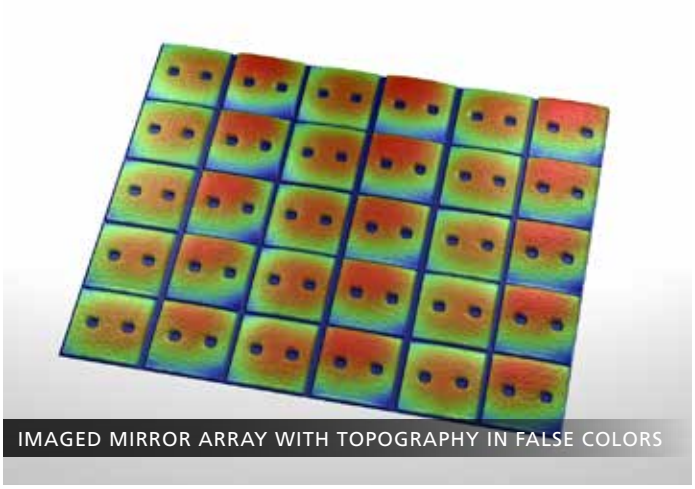
In the framework of a research project aiming the development of energy-saving displays based on silicon micro mirrors, started at Fraunhofer IPMS in April 2009, the research team led by Dr. Christian Drabe worked on the development of a wafer bonding technology which makes the micro mirrors developed at the Institute more energy-efficient. In order to do this, the micro mirrors had to be encapsulated in vacuum, which also meant that four wafers had to be bonded in a stack using vacuum-compatible bonding methods. Because none of the typical adhesives, such as polymers, could be used for vacuum bonding, the so-called anodic and glass frit bonding methods were used. In order to minimize the possible reliability issues of the aluminum metal lines, the bonding temperature had to be kept under 450 °C. After vacuum encapsulation at wafer level was completed, the bonded wafer stack was diced, and the chips were electrical characterized. The resulting chips are approximately 6 mm long, 4 mm wide and 1.6 mm thick. The characterization at chip-level proved that a vacuum of less than 5 mbar was achieved (without getter materials). The obtained vacuum level allowed a reduction of the micro mirror driving voltage from 170 V to 50 V. The driving voltage reduction is a direct proof that vacuum encapsulation at wafer level is an effective way for the reduction of power consumption of actuators based on the electrostatic principle. This research project was part of the Dresden Innovation Center Energy Efficiency (DIZE^{EFF}) and was supported by the European Fond for Regional Development (EFRE), the Sächsische Aufbaubank (SAB) and the Fraunhofer-Gesellschaft. It was run in cooperation with the Faculty of Optoelectronic Components (OES) and the Institute for Packaging of Integrated Electronic Circuits (IAVT) at the TU Dresden.



A MICRO MIRROR CHIP ENCAPSULATED IN VACUUM

IN SITU TOPOGRAPHIC MEASUREMENT OF MICRO MIRROR ARRAYS

The development and optimization of complex micro-opto-electro-mechanical systems (MOEMS) requires a detailed knowledge of the device behavior under application specific operating conditions. In the case of micro mirror arrays, which act as spatial light modulators (SLM) in an imaging system, the flatness of each single mirror affects the image resolution and contrast of the projected image and is therefore a characteristic property of SLMs. In this context, the need for a high resolution surface topography measurement during a laser exposure (in situ) was identified. This measurement complements ex situ characterizations where laser exposure and micro mirror topography measurements are carried out sequentially.



IMAGED MIRROR ARRAY WITH TOPOGRAPHY IN FALSE COLORS

In order to make these measurements, an interferometric setup using the phase-shift principle was designed. The setup combines the highly precise interferometric measurement, allowing a height resolution in the single-digit nanometer range, and the laser irradiation of the SLMs. In general, the setup is neither limited to a specific illumination wavelength nor to micro mirror arrays as a test structure. The influences of different illumination parameters (such as energy density, laser repetition rate, different atmospheres etc.) on the mirror topography can be studied in detail. The results obtained so far give valuable feedback for further technological optimization of the mirror array devices.

SMART-TANK MAKES MONITORING AND OPTIMIZATION OF BIOGAS PROCESSES POSSIBLE

Over the last few years the production of biogas from raw materials harvested from animal husbandry has established itself as a cornerstone in the energy mix of renewable energy sources in Germany. Subsidized by the federal government, this kind of agricultural energy production offers the opportunity to pursue new refinement strategies and to optimize the economic potential of harvests, biowaste and dung from animal husbandry.

The result is an increasing decentralization of energy production: Large, central power plants are being replaced by over 7200 privately run, smaller facilities for power and heat production. A greater need for a cost-effective optimization in the monitoring and controlling of micro-biological processes during the biomass fermentation is the result. Up until now this has been done almost exclusively by measuring the gas volume produced. Sinking gas production, however, usually goes along with long-existing problems within the tank. In time counter-measures are no longer possible, and economic losses are unavoidable.



BIOGAS FACILITY WITH A SMART-TANK PROTOTYPE

With the EU funded project "Smart-Tank" (support code: FP7-SME-2010-1-262241), and in close cooperation with European partners, Fraunhofer IPMS has developed a sensor system for online monitoring during fermentation which uses a probe to measure the indicators relevant to the condition and productivity of the fermenting bacteria. This system puts facility operators in the position to optimize the plants and ensure their stable and reliable operation with the aid of chemical sensors and spectro-analytical procedures. Gas production is held at a constantly high level, and the production is maximized.

UPCOMING EVENTS

Sensor+Test
Nuremberg, Germany
Hall 12, Booth 12-537 May 14 -16, 2013

LASER World of PHOTONICS
Munich, Germany
Hall B2, Booth 421 May 13 -16, 2013

SID Display Week 2013
Vancouver, Canada
Booth 1209 May 21 - 23, 2013

Sensors Expo
Rosemont, IL, USA
Booth 726 June 4 - 6, 2013

SmartSysTech
Erlangen, Germany June 11 - 12, 2013

nanomicro biz
Tokyo, Japan July 3 - 5, 2013

www.ipms.fraunhofer.de/en/events.html

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